3.7.1 Tape Coupler

The Tape Coupler (see Figure 3-12) (P/N 30240-001) occupies backplane slot 7. This board is the interface between the GPF and the mag tape drives. It is interconnected to the other PCB's through the backplane as described in Appendix H. All pins are LOW active unless specified by (H) in the appendix.

The Tape Coupler board does not require jumpers for proper operation in the 4275.

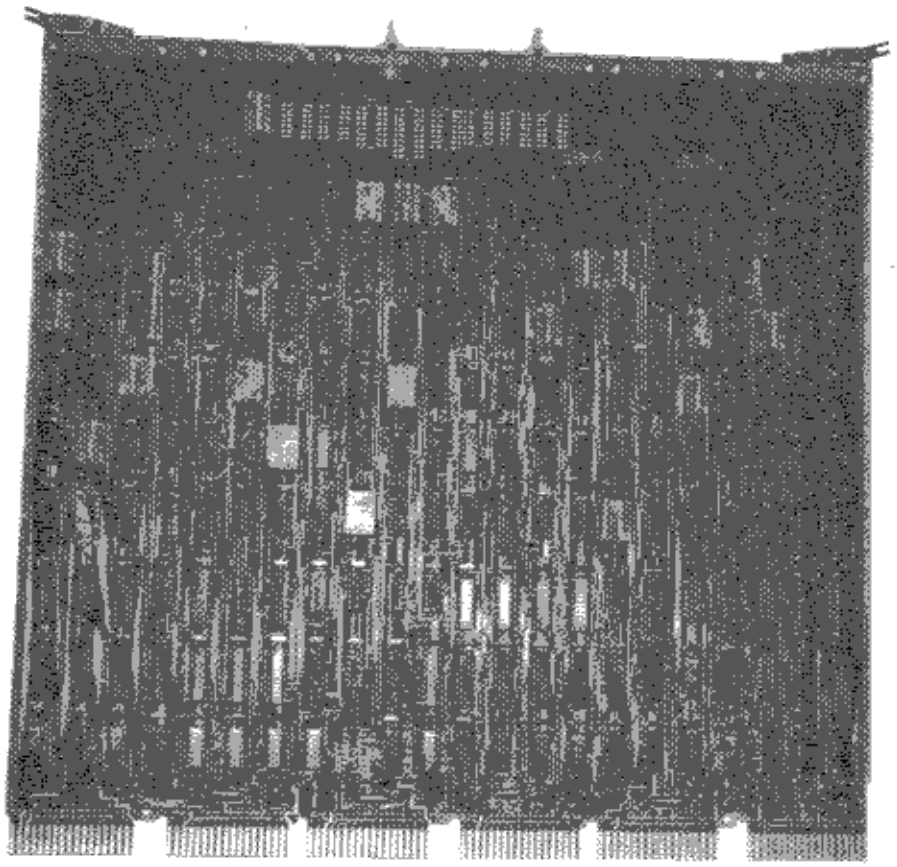


FIGURE 3-12 TAPE COUPLER PCB

3.7.2 Disk Controller

The Disk Controller board (see Figure 3-13) (P/N 31000-001) occupies backplane slot 14. This board is the interface between the GPF and the disk drives. It is interconnected to the other PCB's through the backplane as described in Appendix H. All pins are LOW active unless specified by (H) in the appendix.

The Disk Controller board does not require jumpers for proper operation in the 4275.

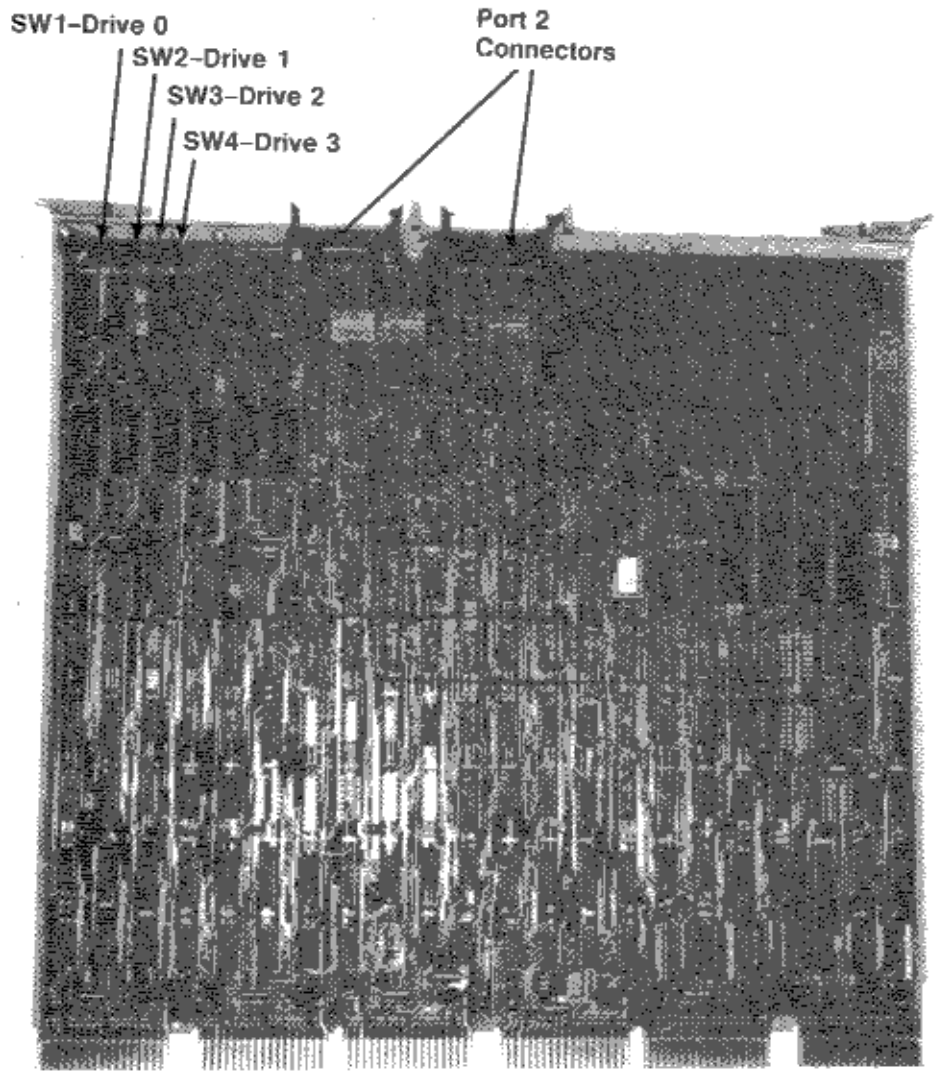


FIGURE 3-13 DISK CONTROLLER PCB

3.7.4.1 HSIL Jumper Connections

Bus request and bus grant levels are determined by jumper connections at location 14A on the HSIL (see Figure 3-16). Normally the HSIL is set to level 4. The following table lists the connections for the various levels. Use this table as a reference only. Do not alter level unless it is incorrect as set by manufacturing.

TABLE 3J HSIL GRANT/REQUEST LEVEL SELECT

Grant/Request Level	Jumper Connections--Location 14A
BR4/BG4	2-5, 3-4, 6-7, 8-9, 10-11, 12-13
BR5/BG5	2-6, 3-7, 4-5, 8-9, 10-11, 12-14
BR6/BG6	2-8, 3-9, 4-5, 6-7, 10-11, 12-15
BR7/BG7	2-10, 3-11, 4-5, 6-7, 8-9, 12-16

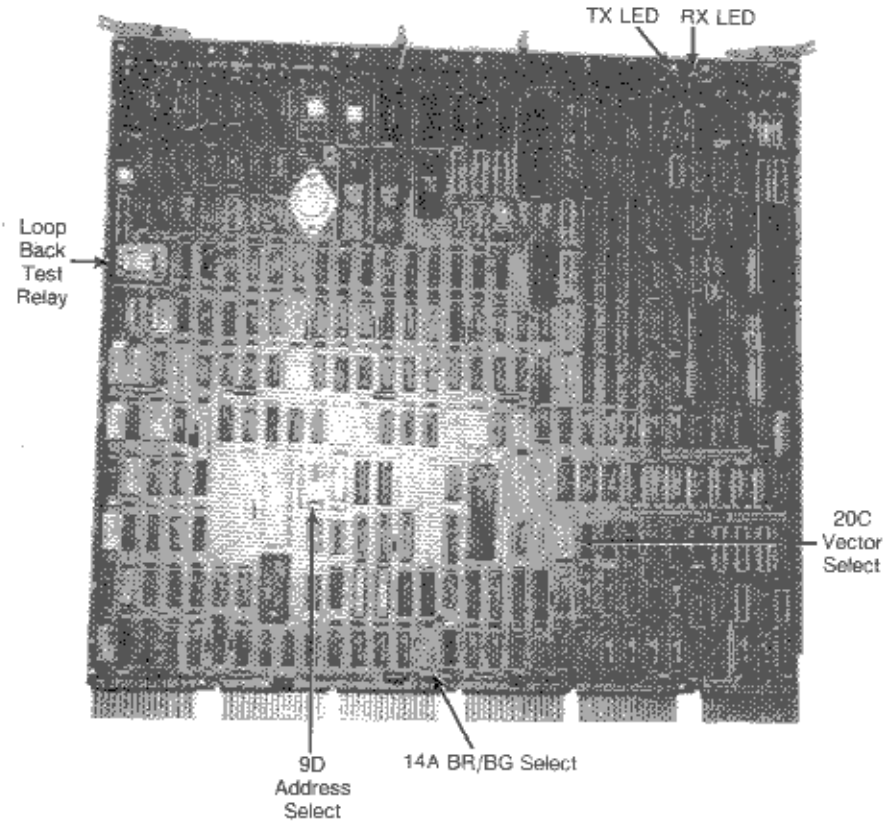


FIGURE 3-16 HOST SERIAL INTERFACE LINK

3.8.1 Intercabinet Cabling

The cabling between the -1 and -2 cabinets consists of an 18ft Unibus cable and several other cables. Intercabinet cabling is shown in Figure 3-3.

3.8.2 Peripheral Equipment Cabling and Connections

3.8.2.1 Disk Controller Interconnection

On the 4275 GPF, a minimum of 300Mbyte of disk storage must be available. This requires the installation of a CDC 300Mbyte drive. This drive as well as all optional drives are attached to the 4275 GPF as follows:

1. Connect the 'A' cable from the first drive to the bottom connector on the disk controller I/O panel.
2. If more than one drive is installed on the system, connect remaining drives in daisy fashion. Install a terminator card in final drive A cable output connector.
3. Connect B cables from attached drives in star fashion to the controller card. Cable of drive 0 connects to bottom B cable connector, drive 1 cable connects to second B cable connector and so forth.
4. Set Disk Controller board rotary switches to appropriate disk sizes for attached drives. SW1, bottom switch on board, determines size of drive 0, SW2 determines size of drive 1 and so forth up to drive 3.
5. Select drive device number on 80Mbyte drives by setting the rotary switch (see Figure 3-18) internal to the drive to the appropriate device number in system (0-4). On 300Mbyte drives, a select plug is used; on 160Mbyte drives a switch-pack located within the drive chassis is used. Device number is dependent on drive position in the daisy chain. First drive is Device 0, second drive is Device 1, and so forth.

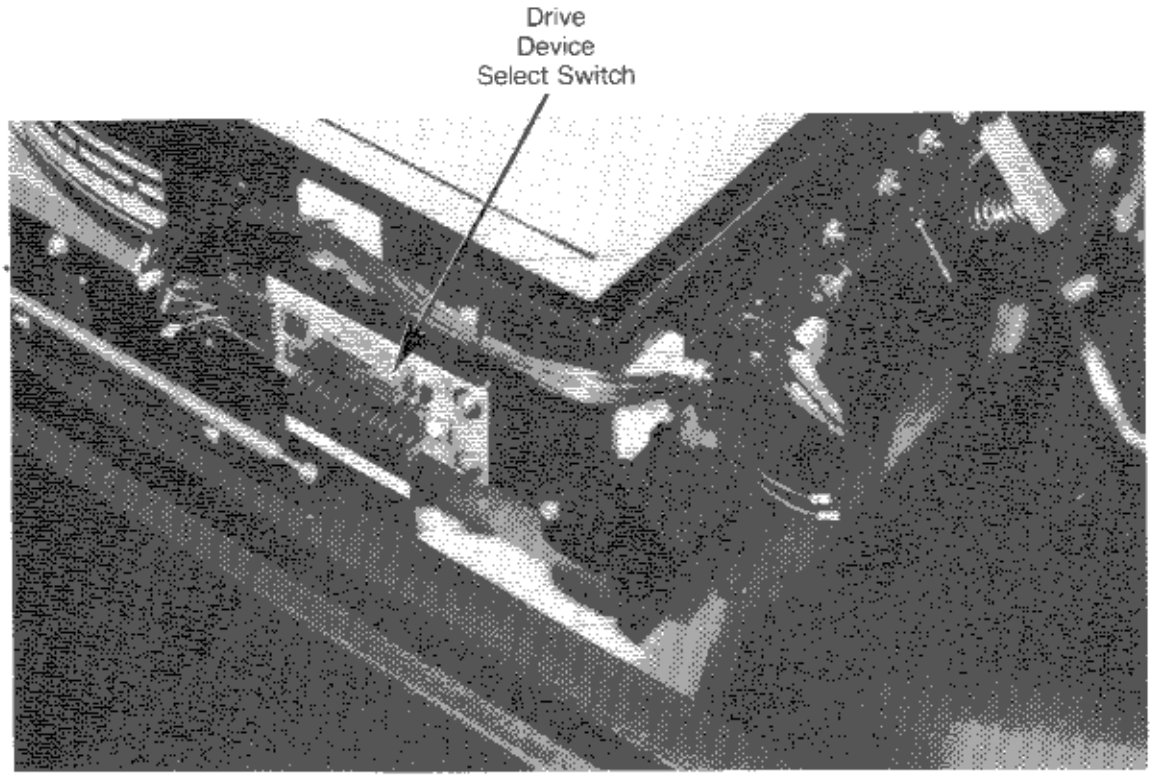


FIGURE 3-18 80MB DISK DEVICE SELECT SWITCH

3.8.2.2 HSIL Interconnection

One HSIL connects the 4275 with up to eight Applicon Graphics Workstations. The HSIL uses two triaxial cables to link the GPF serially with the workstations. Refer to Figure 3-19 for cabling instructions. The last workstation in the chain must have a terminator plug installed in the transmit and receive outputs.

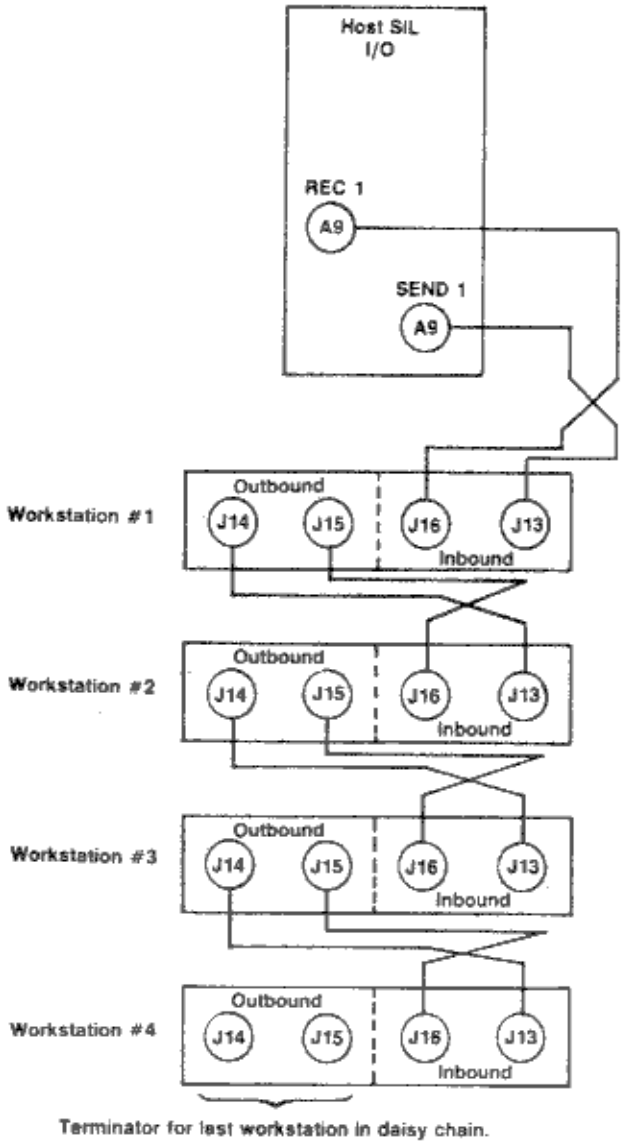


FIGURE 3-19 WORKSTATION INTERCONNECTION

3.8.2.3 MCSI Interconnection

One MCSI connects the GPF with up to four serial peripheral devices. Connections are made between the peripherals and the GPF via eight ModCom connectors located on the MCSI I/O panel. Because there are eight connectors, an optional MCSI can be installed that uses the bottom four 4 connectors. This doubles the number of peripherals that can be attached to the backplane. (See Figure 3-20.)

4.3.2 Disk Controller

The Series 4000 Disk Controller (P/N 31000-001) is a microprocessor-based device designed to interface the GPF with up to four disk drives of various capacities. The controller is a DMA device that links the system disks with main memory in the GPF. Major features of the Disk Controller module are as follows:

1. High-Speed Packet-Driven--data and control information is DMA'ed between the controller and memory in packet format.
2. Overlapped Seeks--the controller supports a maximum of four overlapped seeks. This allows the controller to command all attached drives to seek to a cylinder at one time.
3. On-Board ECC and CRC logic--the controller itself can detect and correct errors of up to 11 contiguous bits. Also, a CRC generator computes the CRC word for writing onto the disk under program control.
4. On-Board Power-Up Diagnostics--At power-up, the controller performs a series of self-tests to ensure proper operation.

The controller can be divided into four main sections: timing logic, 2901 bit-slice processor and associated logic, bus interface logic, and disk interface logic. The following paragraphs provide a general overview of the functions of these three elements. Figure 4-9 is a functional diagram of the Disk Controller.

4.3.2.1 Timing Logic

Timing for controller operations is provided by a 25MHz oscillator and associated clock circuitry. The output of the oscillator is divided down by the logic to provide the clock pulses needed to support controller functions. The microprocessor clock and other clock rates are 200 nsec.

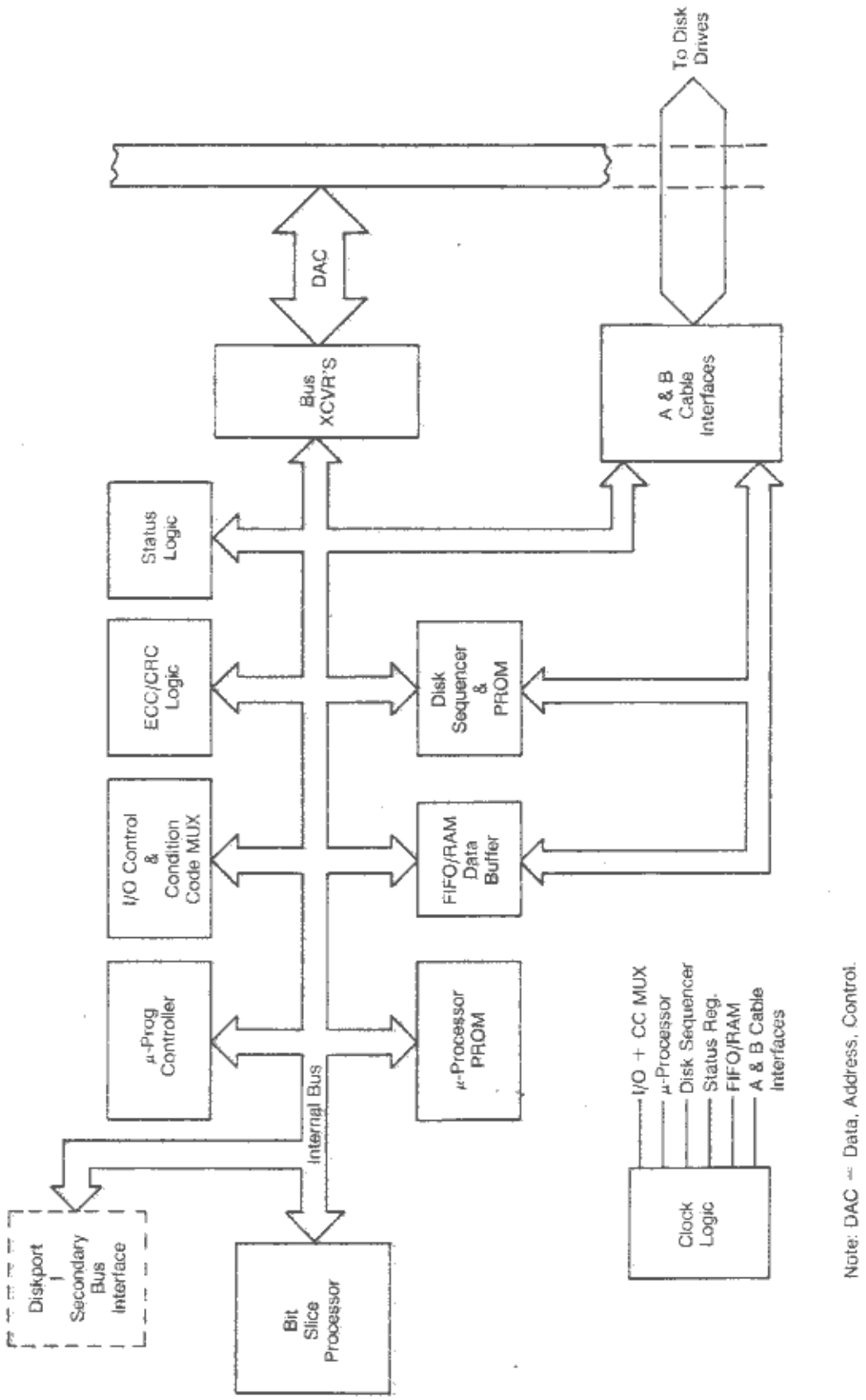


FIGURE 4-9 DISK CONTROLLER FUNCTIONAL BLOCK DIAGRAM

4.3.2.2 Bit-Slice Processor Logic

Functional control of disk controller operations is provided by four 2901 microslice processors and supporting hardware. The 2901's are cascaded together to provide a 16-bit machine. The bit-slice processor functions under control of an on-module microinstruction set. This instruction set is contained in a series of PROM's arranged to provide a 2K by 64 bit program memory.

To control instruction sequences, a 2910 microprogram controller is installed. This IC determines address sequences based on the state of its condition code inputs.

4.3.2.3 I/O Control and Condition Code Logic

I/O control logic consists of eight 3-to-8 decoders and associated gates. Under microcode control, the I/O logic controls data flow to and from the disk controller module and the bit-slice processor. Because the controller is dual-ported, different signal lines are enabled to select one port or the other.

Condition code logic controls the microprogram sequence. Different conditions occurring at different times must be met in order to complete the various processor routines. Five 8-to-1 muxes sample conditions at intervals determined by the microcode. The result of this sampling generates CCEN-H which forces the micro-program controller to advance to the next instruction in the program sequence. As in the I/O logic, certain signals are enabled depending on whether port 0 or port 1 is enabled. A 2 to 1 mux, which is part of the condition code logic, determines port selection based on input from the status logic.

4.3.2.4 FIFO/RAM Disk Data Buffer

All data moving to or from the disk drives pass through the disk data buffer on the disk controller. This buffer consists of four FIFO chips and 4K words of RAM. The FIFO is arranged to form a 16 word by

16 bit device that converts serial data from the disks to parallel data gated into the RAM. The FIFO also converts parallel data from RAM to serial data for transfer out to a disk drive.

The RAM consists of six 2K by 8-bit IC's connected to provide 6K of storage for 16-bit words. This storage area is the disk data buffer. The buffer is structured so that the lower 1K of memory acts as a scratchpad memory for the bit-slice processor. The remaining memory is large enough to ensure that a maximum of sixteen sectors of data (.5 tracks or 4K) can be transferred to and from a disk at one time, if necessary. A buffer of this size greatly reduces disk transfer time (and consequential generation of a DATA LATE signal.)

4.3.2.5 Disk Sequencer and ROM

The disk sequencer logic controls the timing of all disk operations. Because timing is critical in most disk procedures, PROM's are used to ensure proper sequencing occurs. Sector comparator logic is also located in this area of the controller module. This logic compares the specified sector with the physical drive sector and is enabled when a match occurs. Synchronizing logic used to lock the drive signals in step with the controller microcode make up the remaining sequencer devices.

4.3.2.6 Status Logic

Status logic generates reading and writing of the CSR and packet ready information. Power reset logic located here ensures that all CSR bits are reset at power-up.

Fatal hardware error logic indicates a microprocessor malfunction when enabled. As long as the microcode issues a Timeout pulse to this logic, no fatal error signal is generated. Bit 14, RFHE, of the controller CSR allows the resetting of the fatal hardware logic by means of the software. When set, bit 14 also causes the microcode to reset to background loop.

4.3.2.7 ECC/CRC Logic

Built into the disk controller module is the ability to perform error checking and correcting. An ECC shift register generates each sector ECC word when data is written out to the disk. When this same data is read, the controller recomputes sector ECC words and compares them with what was originally written to the disk. If the compare fails, an ECC error occurs and a reread is attempted. If the error cannot be cleared, it is corrected by the controller logic and a soft error is logged. If the error is longer than 11 bits, however, it cannot be corrected and a hard ECC error is generated.

The CRC logic computes the header CRC word and sends it to the disk interface to be written onto the disk. This word is then read by disk logic and compared with the CRC word internally generated by the disk. A successful compare ensures the integrity of the disk data.

4.3.2.8 Primary Bus Interface

The primary bus interface is a series of transceivers and registers used to gate data, address, and control signals between the 11/34 processor and the disk controller. It is designed for compatibility with DEC-standard interface logic. Bus grant and interrupt logic is also a part of the interface. Because the disk controller is a DMA device, logic designed to provide the DMA function for DEC devices is also a part of the interface logic.

4.3.2.9 Disk Interface

The disk controller connects to the associated drives by means of ribbon cables connected to the GPF backplane. The interface logic is CDC standard and as such requires extensive hardware implementation. The signal lines use differential line drivers and receivers requiring -5Vdc inputs. To generate this voltage, the controller requires -15Vdc, which is then regulated down to provide the proper voltage.

Two cables are required to link the controller to a disk drive. These cables are labeled 'A' and 'B'. The 60-pin A cable carries addressing, tag timing, and device status and error data between the drive and the controller. This cable is daisy-chained from drive to drive. The last drive must be properly terminated to ensure correct drive operations.

The 26-pin B cable carries data and timing data between the drives and the controller. Each drive must be individually attached to the controller by a B cable connection. Unlike the A cable daisy chain, the B cables are connected in a radial or star fashion.

4.3.3 Host Serial Interface Link

The Host Serial Interface Link (P/N 30160-001) is a Z80-based module designed to connect the 4275 with up to eight Series 4000 Graphics Workstations. The primary function of the HSIL is the conversion and transmission of data between the GPF and attached workstations. The HSIL transmits data between the two elements at the rate of 1.56 Mbits.

A 32K buffer in the HSIL stores data being transmitted. Access to this buffer is provided by a sequencer chip and related memory logic which function under control of the HSIL Z80. Because the HSIL is a DMA device, data transmitted from a workstation is gated through the buffer into memory with no direct control by the VAX.

Connection to the workstations is via twinax cabling from a backplane I/O connector. To avoid data loss when transmitting, signals are Manchester phase encoded before being placed on the cable. Conversion logic on the HSIL converts NRZ to Manchester, and Manchester to NRZ.

Communications with attached workstations is accomplished by the HSIL using a polling sequence established at power-up. The HSIL uses the polling routine to monitor workstation activity and to acknowledge requests for data transmissions. Two polling lists are maintained by the HSIL. One list contains all active (powered-up) workstations. The second list contains all inactive workstations. The active list is polled at a much higher rate than the inactive list.

Seven 16-bit HSIL registers provide the means of communicating with the VAX and attached workstations. These registers, which provide a bidirectional data and control path between devices, are as follows:

1. Control and Status Register
2. Data Register
3. Status Register
4. Command Register
5. DMA Bus Address Register
6. Word Count Register
7. Terminal Status Register

The HSIL can be divided into six major functional elements as follows:

1. Timing Logic
2. Z80 Processor and Related Logic
3. Bus Interface
4. Sequencer Logic
5. Data Buffer
6. Workstation Interface Logic

The following paragraphs provide a general overview of the functions of each element in the HSIL. Figure 4-10 is a functional block diagram of the HSIL.

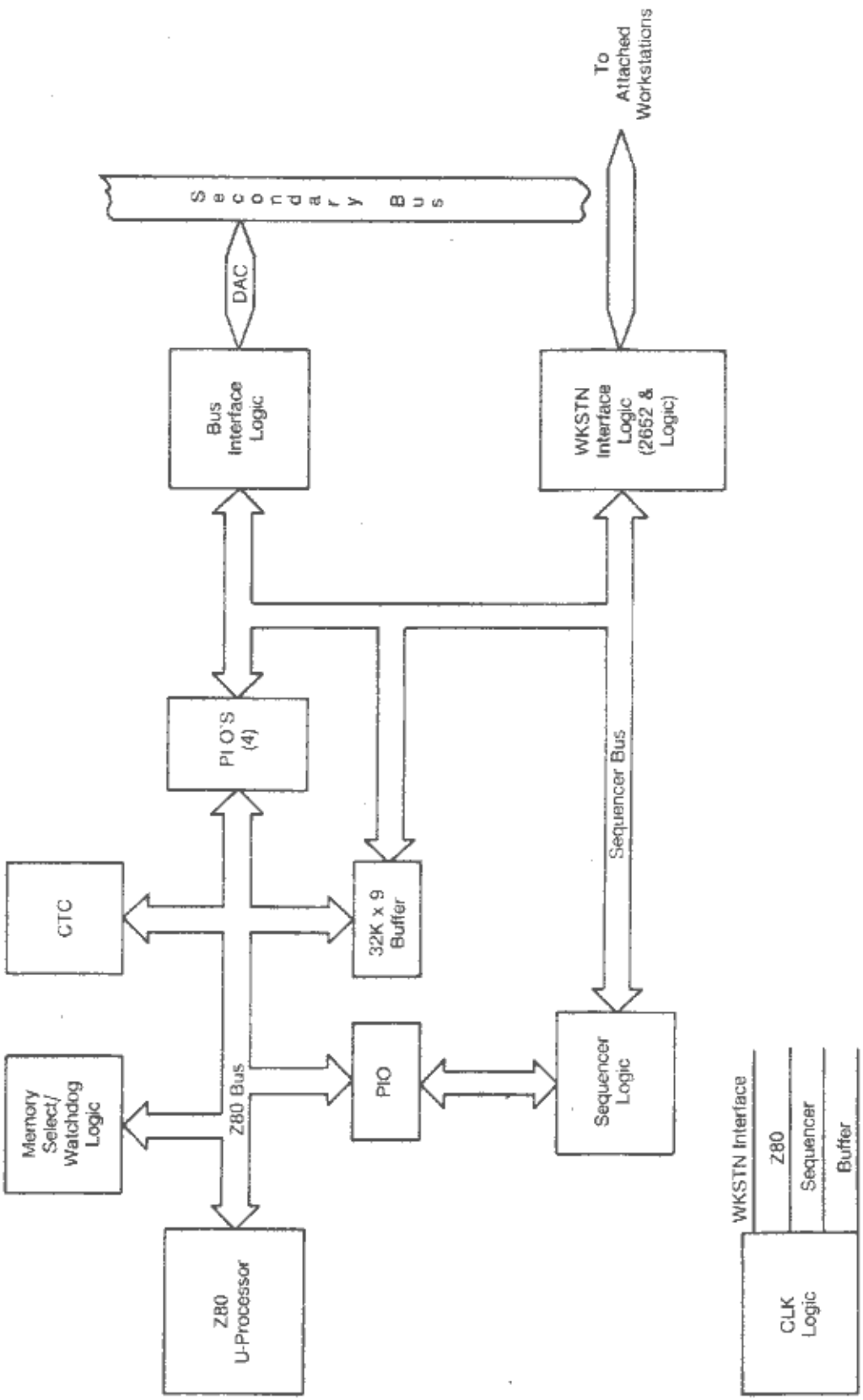


FIGURE 4-10 HOST SIL FUNCTIONAL BLOCK DIAGRAM

4.3.3.1 Timing Logic

A 68.813 MHz oscillator provides initial clocking for the timing logic. A series of divide-down gates and counters provide the necessary clock signals for the HSIL. Critical timing signals include the 4Mhz Z80 clock, RFSHCLOCK for the buffer, and the clocks necessary to convert incoming Manchester encoded data to NRZ format for the GC. These clocks include a 17.2MHz CLOCK58 signal and the 2XCLOCK signal for transmitting data to a workstation.

4.3.3.2 Bus Interface

The Bus Interface contains the logic necessary to connect the HSIL with the unibus. The interface logic consists of the following:

1. Address and Data Transceivers
2. Address Decoding PLA's
3. Bus Address Registers
4. Word Count Register
5. Bus Interrupt and Control Logic

The address and data transceivers allow the HSIL to pass data to and from the bus. They allow for full extended 18-bit addressing and 16-bit word access only (no byte accessing from the bus).

The address PLA decodes incoming addresses from the bus and determines the operations to be performed. The PLA can decode up to any one of 16 base register starting addresses.

The Bus Address Register stores the start address location for memory transfers. It is preloaded at the start of a DMA operation.

The Word Count Register contains the 2's complement of the length of a DMA transfer (number of words transmitted). The HSIL increments the counter at each word transfer. When the register reaches overflow, DMA OFF is generated and the HSIL ends the data transfer.

The bus interrupt and control logic is a standard DEC interface design. It provides the necessary handshaking between the HSIL and the VAX Unibus.

4.3.3.3 Z80 Logic

The Z80 microprocessor and related logic control high level operations within the HSIL. The Z80 manages buffer operations and protocol conventions between the GPF and attached workstations.

Logic associated with the Z80 consists of five PIO's, a CTC, 4K PROM, 2K RAM, and watchdog timer logic. Four of the PIO's perform 16-bit bidirectional data transfers with the Unibus. The fifth PIO links the Z80 with the microsequencer logic. The 4K PROM stores the Z80 instructions; the 2K RAM provides a scratchpad memory for Z80 computations.

The CTC provides timeout functions for the Z80. It also establishes timing necessary for the polling sequences of attached workstations.

The watchdog timer is a 12-bit counter that must be cleared every 32 msec by the Z80. If not cleared , the timer generates a module reset signal causing all HSIL functions to abort. As in other Z80 applications incorporating a watchdog timer, this logic ensures that the Z80 does not become loop-locked or code bound while performing its normal functions.

4.3.3.4 Sequencer Logic

The sequencer controls all data transfers between the HSIL buffer, the Unibus, and workstations. Sequencer logic consists of a 2910 Microprogram Controller, control memory and pipeline registers, and condition code multiplexers.

The 2910 controls addressing of memory based on inputs from the condition code muxes. Memory is PROM-based and contains the code necessary to control data transfer operations. The associated pipeline registers allow one instruction to be gated out of memory while a second instruction is being addressed.

4.3.3.5 Buffer Memory

All data transmitted to and from the HSIL passes through buffer memory. Arranged in a 32K by 9-bit structure, the buffer consists of an address mux, parity check logic, dynamic RAM, and arbitration logic. The buffer can be addressed in three ways: refresh request, necessary because of the dynamic RAM chips used; Z80 request, a standard microprocessor memory access structure; and sequencer controller requests, the most common request.

Of the three types of requests, refresh has the highest priority to ensure data integrity in the RAM. This request is generated by a refresh clock pulse which occurs every eight uSec. Sequencer controller requests have the second highest priority followed by Z80 requests, which occur infrequently.

Arbitration logic resolves priority among the three different memory requests. This logic consists of clock circuitry and decoding logic. When a request occurs, the arbitration logic determines priority and, if no higher request is pending, grants memory access.

4.3.3.6 Workstation Interface

The logic connecting the HSIL with the graphics workstations consists of a 2652 Multi-Protocol Communications Controller (MPCC) transceiver, Manchester encoding and decoding logic, transmit and receive LEDs, and two 16-bit registers. The MPCC operates under microcode control from the sequencer.

The MPCC is a parallel-to-serial converter. It also performs CRC and error checking functions on data being processed. A transceiver at the parallel interface permits two-way transmission of data.

A 16-bit receive register located after the transceiver allows data to be gated to the memory buffer in 2-byte increments. A second 16-bit transmit register allows 16 bits of buffer data to be passed to the 8-bit transceiver in 1-byte increments.

The encoding/decoding logic within the interface converts outgoing NRZ data to Manchester encoding for transmission to the workstations. Decoding of incoming Manchester-encoded data from the workstations is also performed here.

Manchester encoding is employed because of the cable lengths used to connect workstations to the GPF. Converting NRZ data to Manchester allows the data to be transmitted greater distances, and allows the use of ac coupling to eliminate ground loops. Converting NRZ to Manchester requires mixing serial data with a clock signal and transmitting the result via line drivers onto the cable.

Converting Manchester data to NRZ requires a decoder that synchronizes the incoming signal and passes it through a differentiator to extract data and clock signals. In this conversion process timing signals are critical to the extraction of data.

The transmit and receive LEDs light whenever data is present on the associated signal lines. The incoming serial data line is tapped before the MPCC and fed to a one-shot whose output causes the Receive LED to light when data is sensed. The serial transmit lead is tapped in a similar fashion to provide a signal to the Transmit LED.

4.3.3.7 HSIL Addresses

Following is a list of HSIL registers and associated addresses.

ADDRESS	REGISTER
766140	HSIL #1 CSR
766142	Data
766144	Command
766146	DMA Bus Address
766150	Word Count
766152	Terminal Status

4.3.4 Tape Coupler

The Tape Coupler module (P/N 30240-001) standard in the Model 4245 interfaces the GPF with up to four interconnected tape drives. Various combinations of drives can be connected to the coupler, which can accommodate speeds up to 75 ips and either 800 or 1600 BPI density. The coupler is a DMA device that transmits data between the GPF and attached drives.

The coupler consists of a series of registers, control logic, and bus interface logic. Unlike other controller modules in the Series 4000 GPF's, the coupler module contains no microprocessor and supporting code. The coupler merely provides the timing and interface logic necessary to transmit data to and from the tape drive. A 64 word by 8-bit FIFO acts as a buffer for data passing through the coupler.

Figure 4-11 is a functional representation of the Tape Coupler module. Major components of the coupler are as follows:

1. Timing and Control Logic
2. Register Logic
3. Bus and Formatter Interface Logic
4. FIFO Logic

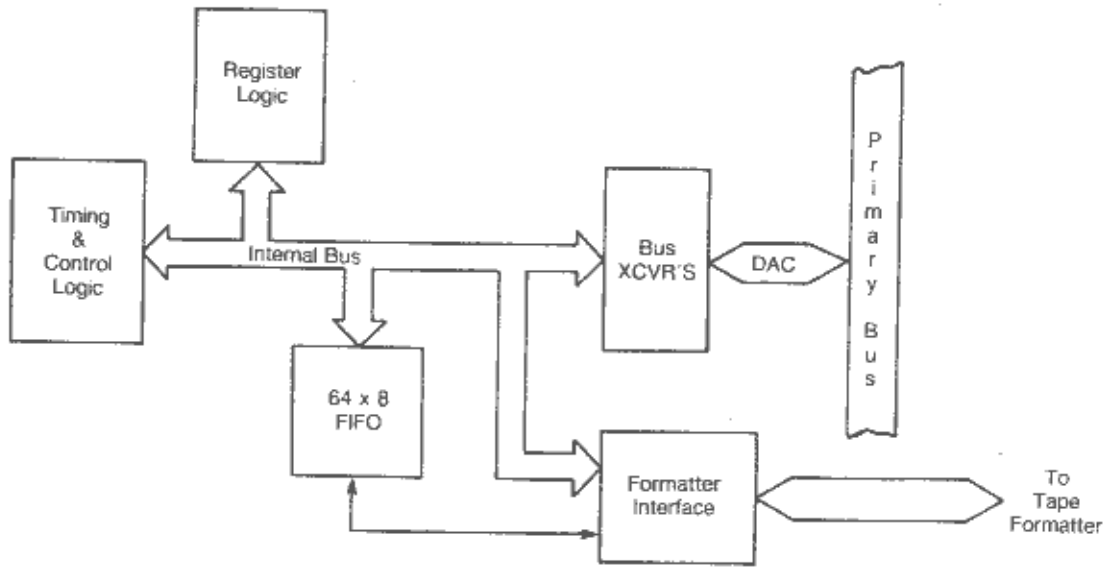
4.3.4.1 Timing and Control Logic

Spread throughout the coupler, the timing and control logic ensures that critical signals are properly routed through the modules. The timing logic also ensures that data transfer operations occur in the proper sequence. Control functions include command decoding, status monitoring, and data transfer synchronization. Proper timing is achieved by delay gates and clock flip-flops on the coupler module.

4.3.4.2 Register Logic

The Tape Coupler register logic consists of eight registers and associated circuitry. These registers are addressable by the VAX 11/751 processor and provide the various command and control signals for coupler and tape formatter operations. The eight coupler registers are as follows:

1. Mag Tape Status (MTS)--766040--A 16-bit read-only word addressable register cleared by BUSINIT, PCLR, or a command word. The MTS provides status information on the mag tape drive for the coupler.
2. Mag Tape Command (MTC)--766042--A 16-bit read/write register, either byte or word addressable, used by the 11/34 to control coupler operations.
3. Mag Tape Byte/Record Count (MTBRC)--766044--A 16-bit read/write register used to count bytes during read or write operations. It is also used to count records during space forward and reverse operations. The MTBRC register is byte or word addressable.
4. Mag Tape Current Memory Address (MTCMA)--766046--A 16-bit counter that contains the 16 least significant bits of the memory address for non-processor request read and write data transfers. MTCMA is preset with the address where the first character read or written will be located. Bits 16 and 17 of the current memory address are stored in the MTC.



Note: DAC = Data, Address, Control

FIGURE 4-11 TAPE COUPLER FUNCTIONAL BLOCK DIAGRAM

5. Mag Tape Data (MTD)--766050--Two 16-bit holding registers used for data transfers during read/write operations.
6. Mag Tape Read Line (MTRD)--766052--A 16-bit read-only register used for error checking. Not used in Series 4000 applications.
7. Mag Tape Option 1 (MTOP1)--766054--A 16-bit read/write register used for maintenance purposes only.
8. Mag Tape Option 2 (MTOP2)--766056--A 16-bit read/write register used for maintenance purposes only.

4.3.4.3 FIFO Logic

The 64 word by 8-bit FIFO buffers data from the primary bus and gates it out to the tape transport. The FIFO also performs the reverse function on data coming from the tape. The coupler uses the FIFO to hold data from the bus until synchronization with the tape formatter is achieved. Using the buffer in this application limits the occurrence of bus latency problems in the system.

4.3.4.4 Bus Interface Logic

The bus interface is a series of transceivers and registers used to gate data, address, and control bits between the coupler and primary bus. This logic includes bus request, bus grant, master and slave synchs, and npr information. Because the coupler is a DMA device, the NPG signal is routed to it. The basic structure of the interface is based on DEC-standard logic.

4.3.4.5 Formatter Interface

The coupler connects to the tape formatter through two backplane I/O panel connectors attached to a pair of 50-pin cables. Interface logic consists of registers and line drivers that gate data and control signals to and from the formatter.

4.4 11/751 TIMING

Timing circuitry on the 11/751 is designed to execute micro-instructions at a 320nSec rate. CPU/Memory Interconnect (CMI) bus transactions are synchronized by a 160nSec clock. The timing necessary for these clock pulses is derived from an 18.75Mhz crystal oscillator within the VAX CPU.

Located on the CCS, the 18.75Mhz crystal oscillator generates the basic signal for clocking throughout the VAX. The Service Arbitration and Control (SAC) gate array on the DPM module takes the 18.75Mhz signal and generates CPU timing. One of the SAC outputs is a non-symetrical 6.25Mhz waveform which is the time base for the VAX system. This signal is called BASE CLK and has a period of 160 nSecs.

Timing signals generated by SAC from the BASE CLK include B CLK, bus clock; M CLK, microsequencer clock; D CLK, destination clock; and PHASE clock. B CLK, 160nSecs in width, synchronizes bus activities on the CPU Memory Interconnect (CMI) bus. M CLK, 320nSec, clocks new microinstructions into the DPM. D CLK, also 320nSec, clocks data to the scratchpads and registers at the end of a microinstruction. PHASE clock is a symmetrical waveform 320nSecs long. It divides the microinstruction into two parts for testing at mid-microcycle time.

The clock periods for M CLK, D CLK, and PHASE can be stretched beyond the normal periods by the microsequencer depending on CPU state. Also, these signals are confined to the four CPU modules. B CLK is distributed throughout the system via the CMI. Table 4J lists the various clock signals and their backplane pin locations.

TABLE 4J MAJOR CLOCK PULSES

Signal Name	Slot #	Pin #
CPU OSC OUT H	L0005	B31
CPU OSC OUT H	L0002	B28
CPU OSC IN H	L0002	B27
BASE CLK L	L0002	A73

TABLE 4J MAJOR CLOCK PULSES (cont'd)

Signal Name	Slot #	Pin #
B CLK L	L0002	B9
M CLK L	L0002	B5
D CLK ENABLE H	L0002	B25
M CLK ENABLE H	L0002	B15
PHASE 1 H	L0002	A78

4.5 11/751 BUS STRUCTURE

As can be seen in Figure 4-1, there are four main buses in the VAX CPU. These are discussed in the following subsections. A detailed discussion of buses internal to the various modules is beyond the scope of this document.

The four major VAX buses are the CMI, the Unibus, the MBus, and the WBus. These four buses link all major system components allowing the transfer of address, data, and control signals between various modules within the 4275 GPF.

4.5.1 CMI Bus

The CPU/Memory Interconnect (CMI) is a backplane communications bus consisting of 45 bidirectional lines that carry address, data, and arbitration signals between modules on the VAX backplane. The CMI extends from slot 3 (MIC) to slot 10 (CMC). It is etched entirely on the backplane and has no cables or connectors other than the module sockets. It is not intended to be extended beyond its present length.

All modules connected to the CMI are synchronized to B CLK from the DPM. A master/slave relationship is established between modules on the CMI and no other transactions can take place until the previous one completes. All data transactions are 4 bytes in length.

CMI signals are divided into four groups: bus clock (B CLK), data/address and control, priority arbitration, and status. Table 4K lists and defines signals that make up these four groups. Table 4L lists and defines CMI priority levels.

TABLE 4K CMI SIGNALS

Group	Signal Name	Description
TIMING	B CLK L	160nSec pulse used to synchronize bus activity.
DATA/ ADDRESS AND CONTROL	CMI DATA (31:00)	Asserted by bus master which then transmits control and address information. Lines are then enabled to transfer data.
	DBBZ	Data Bus Busy is asserted by master for one cycle while it places the CMI address on the data lines. The slave then asserts DBBZ until transfer is complete. Does not occur during a write to slave because the slave is immediately ready to accept data.
	HOLD	Used to temporarily suspend CMI activity.
	WAIT	Asserted to initiate a processor interrupt by a unibus device. Held until write vector operation is performed.
PRIORITY ARBITRATION GROUP	ARB7-ARB1	A level (7 to 1) is assigned to each device capable of becoming a bus master on the CMI. Highest priority is given to device with highest ARB number (ARB7). See Table 4L for arbitration structure.
STATUS GROUP	ST1, ST0	Transmitted by a slave to indicate status of transaction to CMI master. Indicate success or failure of transaction. Bit interpretation is as follows: ST1 ST0 INTERPRETATION 0 0 Non-existent memory 0 1 Non-correctable error 1 0 Corrected data 1 1 No errors

TABLE 4L CMI PRIORITY LEVELS

Priority Level	Module Name	Comment
ARB7	MTM	Maintenance Test Module (L0006)
ARB6	Reserved	Not used at present
ARB5	Reserved	Not used at present
ARB4	UBI	UNIBUS INTERFACE Module (L0004)
ARB3	Option	Not used (Mass Bus Adapter 0 or UBI 1)
ARB2	Option	Not used (MBA 1)
ARB1	Option	Not used (MBA 2)
NONE	CPU	CPU has no priority. It uses bus when all others are finished.

4.5.2 Unibus

The Unibus architecture in the VAX is identical to that of DEC PDP11 processors. The Unibus provides the communications link between the VAX CPU and Unibus I/O controllers. It is composed of 56 signal lines grouped logically into three sections as follows. (Refer to Table 4M for Unibus signals.)

1. INITIALIZATION (3 lines)--controls power-up/down and bus device initialization sequencing.
2. DATA TRANSFER(36 lines)--carries data and address information between devices.
3. PRIORITY ARBITRATION (15 lines)--determines device priority for Unibus access.

TABLE 4M UNIBUS SIGNALS

Active State	Signal Name	Description
L	INIT	Asserted by UBI when DCLO asserted on unibus. Remains asserted for 70msec following DCLO negation.
L	ACLO	Warns of impending power failure. Initiates the power-fail trap sequence.
L	DCLO	Asserted when an out-of-voltage condition occurs. Available from each power supply.
L	A17:A00	Address lines enabled by the master device to select a slave. A17-A01 addresses a 16-bit word, A00 specifies a byte within the word.
L	D15:D00	Data lines transfer data between master and slave devices.
L	C1:C0	Control lines are coded by the bus master to control the slave in one of four transfer operations as follows: C1 C0 TRANSFER OPERATION 0 0 DATI--Data word to master 0 1 DATIP--DATI followed by DATO or DATOB 1 0 DATO--Data word to slave 1 1 DATOB--Data byte to slave
L	PA:PB	Transfer parity information from slave to master during DATI operation as follows: PA PB INTERPRETATION 0 0 No error 1 0 Parity error 0 1 Reserved 1 1 Reserved

TABLE 4M UNIBUS SIGNALS (cont'd)

Active State	Signal Name	Description
L	MSYN	Master synchronization asserted by the master to indicate valid data and address information on the bus to the slave during a DATO or DATOB operation.
L	SSYN	Slave synchronization asserted by the slave to indicate write data has been clocked on a DATO or DATOB operation. On a DATI or DATIP operation, indicates that the slave has asserted READ data to the master.
L	NPR	Non-Processor Request is issued by an I/O device for a DMA transfer that does not require processor intervention.
H	NPG	Non-Processor Grant in the response by the processor to an NPR. Indicates that the device request has been granted.
L	BR7:BR4	Bus Request from an I/O device for an interrupt operation.
H	BG7:BG4	Bus Grant from the processor in response to the bus request from the device having the highest priority.
L	SACK	Select Acknowledge is asserted by a bus requesting device which has received a processor grant. Bus control passes to this device when the current master completes its operation.
L	BBSY	Bus Busy indicates that the Unibus is presently in use. Asserted by the bus master until transaction completion.
L	INTR	Interrupt is asserted by an interrupting device having received a bus grant signal. INTR is cleared upon receipt of SSYN from the UBI at transaction end.

4.5.3 MBus

The MBus consists of 32 tri-state data lines that are under microcode control. It is a major communications bus between the DPM, MIC, and optional FPA modules. The MBus operates entirely under control of the microcode. Data from the following sources can be gated onto the MBus: MTEMPs, Write Data Register (WDR), Memory Data Register (MDR), Virtual Address Register, Execution Buffer, PC Backup Register, Memory Address Register, Translation Buffer. See Figure 4-12.