MDB/MLSI-DWQ11

BUS INTERPRETER

For use with DEC™ LSI-11™ PDP-11™
and VAX™ Computers

INSTRUCTION MANUAL

MDB SYSTEMS, INC.

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SECTION ONE
GENERAL DESCRIPTION

1.0 Introduction

This is an instruction manual for the MDB Systems' Bus Interpreter Assembly (designated the MDB/MLSI-DWQ11) to be used with Digital Equipment Corporation (DEC) PDP-11 Unibus, VAX, and LSI-11 Q-bus computers.

This manual provides instructions and information for installing, programming, and utilizing the MDB/MLSI-DWQ11. Assembly drawings and schematic diagrams are also provided to facilitate routine user maintenance and repair.

The MDB/MLSI-DWQ11 will hereafter be referred to, for brevity, as the Bus Interpreter.

Before constructing a system in which to utilize the Bus Interpreter, it is highly recommended that the user become familiar with the bus architecture and operational characteristics of the PDP-11 Unibus and the LSI-11 Q-bus. For detailed information concerning the Unibus and Q-bus, refer to the following DEC documents:

- PDP-11 Processor Handbook and/or PDP-11 Architecture Handbook
- PDP-11 Peripherals Handbook
- PDP-11 Terminals and Communications Handbook
- Microcomputers and Memories and/or Microcomputer Processor Handbook

1.1 General Description

The Bus Interpreter Assembly consists of one quad-size MDB-DWQ module, one dual-size MLSI-DB11 module, and three 10-foot (3.05m) flat ribbon interconnection cables. When installed, the Bus Interpreter performs one of the following user-selected functions:

1. Permits a PDP-11-based Unibus system to utilize less expensive and more compact Q-bus compatible memories and controllers. The PDP-11 processor performs all bus arbitration.

   When an MDB Systems' Q-bus Switch Assembly (MLSI-DB11-S) is used along with the Bus Interpreter, it permits a PDP-11 system to share Q-bus peripherals with several other LSI-11 Q-bus systems.

2. Permits an LSI-11-based Q-bus system to utilize Unibus compatible memories and controllers. The LSI-11 processor performs all bus arbitration.

The illustrations below are simplified block diagrams of the Bus Interpreter as it is typically installed in a PDP-11 Unibus system, and in an LSI-11 Q-bus system.

Figure 1-1
Block Diagram: Bus Interpreter (Unibus Main System)

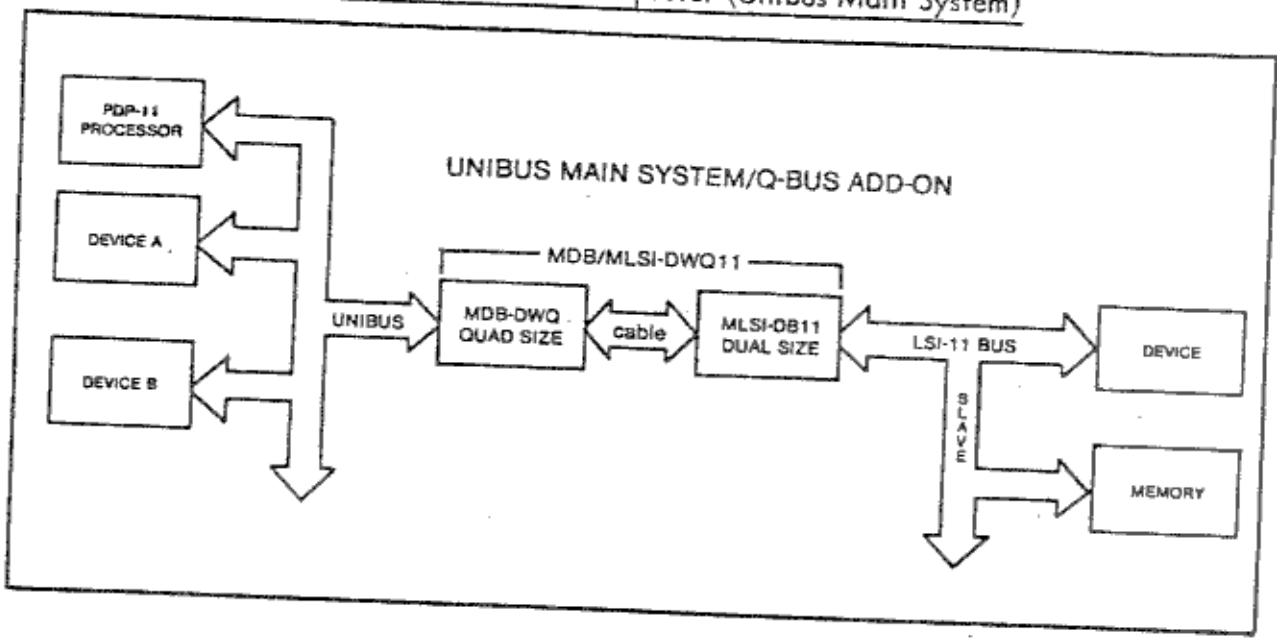


Figure 1-2
Block Diagram: Bus Interpreter (Q-bus Main System)

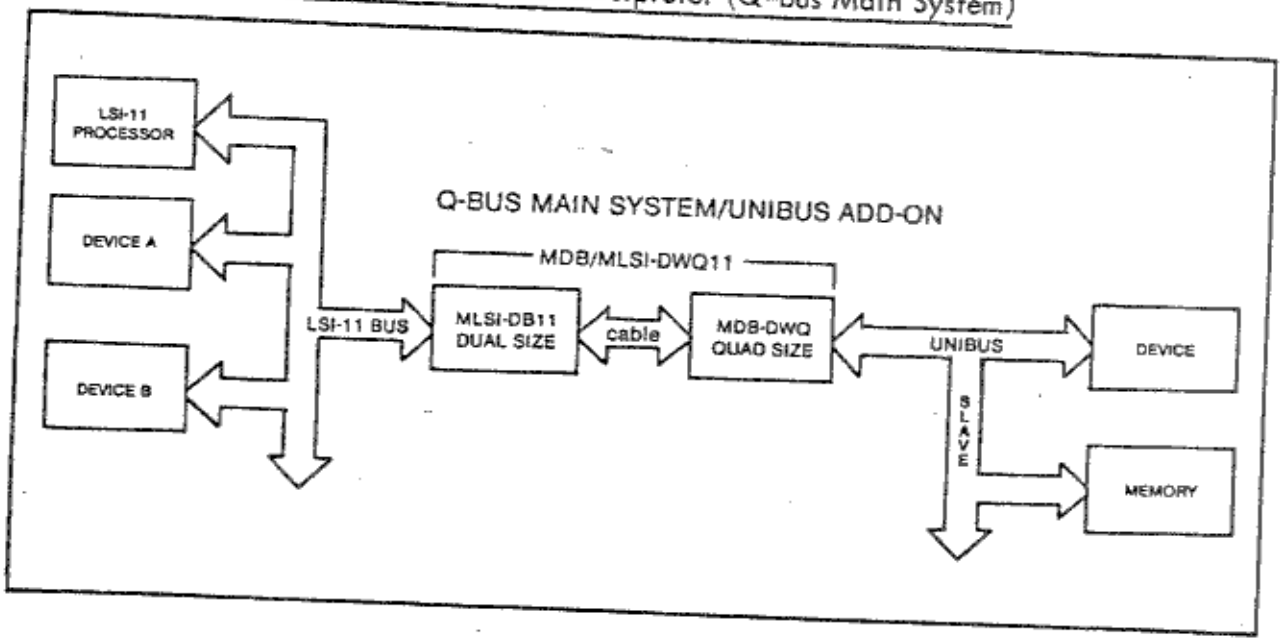
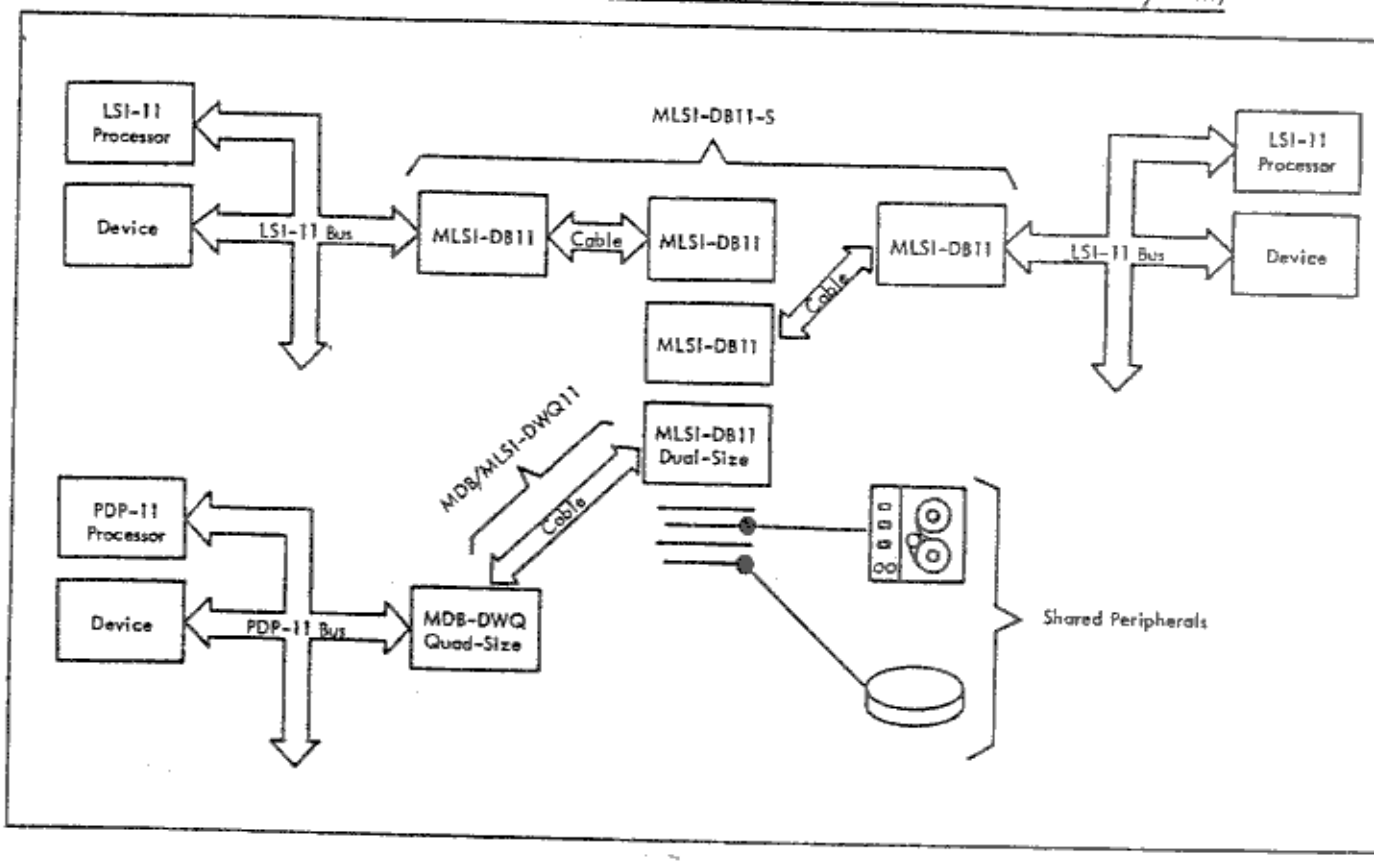


Figure 1-3 shows the Bus Interpreter installed in a multi-processor system which utilizes an MDB Q-bus Switch Assembly (an MLSI-DB11-SA is shown). The Bus Interpreter also acts as a Q-bus switch and allows the processors to share common peripherals residing on the "shared" bus.

Figure 1-3
Block Diagram: Bus Interpreter and Q-bus Switch (Multi-Processor System)



1.2 Features

Features of the Bus Interpreter include:

- DMA transfers are supported across the Interpreter in both directions.
- Supports 22-bit addressing.
- Implements the 4-level priority interrupt structure of the PDP-11 Unibus and the LSI-11/23 Q-bus processors.
- Devices on the "add-on" bus may be assigned a higher or lower DMA and serial interrupt priority than devices on the main system.
- Accommodates 4 megabytes of memory, including the I/O page, on LSI-11/23 Q-bus systems. (When Unibus memory devices are used, only 256 K bytes of memory may be accessed.)
- Supports memory parity for both Q-bus and Unibus memories.
- Compatible with Unibus "Grant Steal" cycles.
- Has the capability to drive an additional 19 DC bus loads on the "add-on" bus.
- Depending upon placement in the system, has the capability to provide 120 ohm termination in each system segment.
- Seven edge-mounted LED's indicate Power On, type of main processor (Q-bus or Unibus), Bus Master, and interrupt status.
- Software transparent to the host computer.
- Permits the "sharing" of computer resources (including Q-bus peripherals) through its Bus Switch capabilities. Can be networked into multi-processing arrays.
- Provides "isolation." When the Bus Switch section is turned "off," the CPU may be disconnected from the multi-processor system without affecting the operation of the other CPU's or the shared bus.

1.3 Specification Summary

1. Mechanical

a. Logic Modules: One (1) quad-size MDB-DWQ module (45040270).

One (1) dual-size MLSI-DB11 module (45040267).

b. Interconnection Cables: Three (3) 10-foot (3.05m) GPRCSR-D flat interconnection cables, as follows:

1. 60-pin (p/n 50046856-XXX)
2. 26-pin (p/n 50046852-XXX)
3. 10-pin (p/n 50046850-XXX)

c. LED Indicators: Seven (7) edge-mounted LED's on the MDB-DWQ module indicate the following:

1. Power On (ON)
2. Q-bus CPU (Q CPU)
3. Unibus CPU (U CPU)
4. Q-bus Bus Master (Q BM)
5. Unibus Bus Master (U BM)
6. Q-bus interrupt to Unibus CPU (Q-U I)
7. Unibus interrupt to Q-bus CPU (U-Q I)

One (1) edge-mounted LED on the MLSI-DB11 module indicates "Module On," or "ACTIVE."

d. Jumpers: Jumper 3 F-H in location 11/12 E on the MDB-DWQ determines the type of system CPU used. 3 F-H is removed for a Unibus CPU, and installed for a Q-bus CPU. (Factory-removed.)

Jumpers 1 F-H, 2 F-H, 3 F-H, and 4 F-H in location 3/4 E on the MLSI-DB11 module are installed in all configurations.

(For a complete listing of jumper configurations, refer to Section Two: Installation.)

e. Switches: An eight-position DIP switch in location 6E on the MDB-DWQ module is used for the selection of an interrupt vector address for Unibus devices which execute "Grant Steal" cycles when used with an LSI-11 CPU.

2. Electrical

a. Power Required: The MDB-DWQ requires +5V DC at 4.0 amps.

The MLSI-DB11 requires +5V DC at 2.5 amps.

b. Bus Loading: The entire Interpreter Assembly places one (1) DC bus load on the primary CPU system bus.

The Interpreter has the capability to drive an additional nineteen (19) DC bus loads on the "add-on" bus.

SECTION TWO
INSTALLATION

2.0 General

The Bus Interpreter Assembly consists of a quad-size module (MDB-DWQ) that plugs into a standard peripheral (SPC) slot of a Unibus backplane, a dual-size module (MLSI-DB11) that plugs into a Q-bus backplane, and a cable set consisting of three 10-foot (3.05m) interconnection cables.

The Interpreter can be inserted into any slot of the "main system" (either Unibus or Q-bus), with other interfaces or memories located ahead of, or behind the Interpreter. The "main system" contains the CPU.

Devices which are installed in the "add-on" bus can be assigned higher or lower DMA and serial interrupt priority than other devices on the "main system."

Note: The Interpreter module which is installed in the "add-on" bus is always inserted into the first slot of that backplane.

Before installing the Interpreter, decide whether or not you want the devices on the "add-on" bus to be of higher priority than any particular device on the "main system." If you do, perform the installation procedures described in the following paragraphs that pertain to your CPU type for the "Interpreter not at the end of the bus" phase. Insert the Interpreter module that is dedicated for the "main system" backplane just ahead of the device you wish to have lower priority than the devices on the "add-on" bus.

The following paragraphs provide instructions and information for installing the Bus Interpreter in one of four possible configurations, as follows:

1. Unibus CPU with the Bus Interpreter at the end of the Unibus.
2. Unibus CPU with the Interpreter NOT at the end of the Unibus.
3. Q-bus CPU with the Interpreter at the end of the Q-bus.
4. Q-bus CPU with the Interpreter NOT at the end of the Q-bus.

The Interpreter may also be used in a "Bus Switch" configuration. Refer to Section Three: Interpreter/Switch Control Combinations, for additional information.

Note: In all configurations listed above, jumpers 1 F-H, 2 F-H, 3 F-H, and 4 F-H are installed on the MLSI-DB11 module. Additional required jumper configurations for each Interpreter system are listed in the following paragraphs.

2.1 PDP-11 Unibus CPU

The paragraphs below describe installation procedures for the Interpreter when it is used with a PDP-11 CPU system.

2.1.1 Interpreter at the End of the Unibus

To install the Bus Interpreter at the end of the bus occupied by the PDP-11 CPU, perform the following steps:

1. Install jumper 5K-6K in location 6E on the MLSI-DB11 module, and remove jumpers 5F-6F, 5H-6H, and 5L-6L. In addition, resistor packs should be installed on the module at locations 3A, 7A, and 6C to provide the necessary bus termination in the event that a Unibus Terminator module is not used.

2. Install jumpers 1 F-H and 2 F-H in location 9E on the MDB-DWQ module, and remove jumpers 3 F-H and 4 F-H.

3. Remove the NPR backplane jumper (pins CA1 to CB1) from the last slot of the Unibus backplane.

4. Insert the MDB-DWQ module in the last Unibus backplane slot.

5. Insert the MLSI-DB11 module in the first slot of the Q-bus backplane. (The Q-bus CPU cannot be used in this configuration.)

6. Connect the 10-foot (3.05m) 60-pin interconnection cable between connector P1 of the MDB-DWQ module and P1 of the MLSI-DB11.

7. Connect the 10-foot 26-pin cable between P2 of the MDB-DWQ and P2 of the MLSI-DB11.

   Note: The 10-pin cable is not used in a Unibus CPU configuration.

8. When the system is "powered on," the LED on the edge of the MLSI-DB11 module should illuminate to indicate module ACTIVE. On the MDB-DWQ, the ON, U CPU, and U BM LED's (when used) should also illuminate upon power-up.

For a detailed diagram of cable connections, refer to Installation Drawing 01034004, contained at the end of this instruction manual.

For "bus switching" details, refer to Section Three of this manual.

2.1.2 Interpreter NOT at the End of the Unibus

To install the Bus Interpreter in the bus occupied by the PDP-11 processor, but NOT at the end of that bus, perform the following:

1. Perform all installation procedures outlined in paragraph 2.1.1, with the exception of Step 3.

2. Remove the NPR jumper (CA1 to CB1) from the Unibus SPC slot in which the MDB-DWQ module is to be installed.

3. Remove all resistor packs (SIP and DIP) on sockets from the MDB-DWQ module. This prevents double termination of the Unibus.

In this configuration, the MDB-DWQ module may be installed in any available SPC slot in the Unibus.

2.2 LSI-11 Q-bus CPU

The following paragraphs describe installation procedures for the Bus Interpreter when it is used with an LSI-11 CPU. Also provided is a description of the capability of Unibus DMA controllers to "steal" bus grants when used with an LSI-11-type CPU.

2.2.1 Grant Steal Interrupt Vector

Unibus DMA controllers which employ "interrupt grant steal" circuitry for minimal DMA latency may be used in the "add-on" bus, as the Interpreter will sense a "Grant Steal" Unibus cycle and convert it to a compatible Q-bus cycle which the LSI-11 CPU can arbitrate and complete.

The Unibus DMA controller accomplishes this through the Bus Interpreter by causing an interrupt to the Q-bus CPU in the vector space which is automatically filled between the top of the assigned vector space and the bottom of the stack ("Non-Sense Interrupt Vectors"). "Auto-filling" is done by RSX and RT-11 during the SYSGEN, which writes RTI's to the vector space.

The interrupt is completed by the LSI-11 CPU as a Return from Interrupt (RTI) and the system continues to the next instruction and the next bus cycle.

If you are using any Unibus DMA controllers which contain the "Grant Steal" feature, determine the RTI vector area (non-sense vector) from the SYSGEN and set the DIP switch pack in location 6E on the MDB-DWQ module to the corresponding vector location.

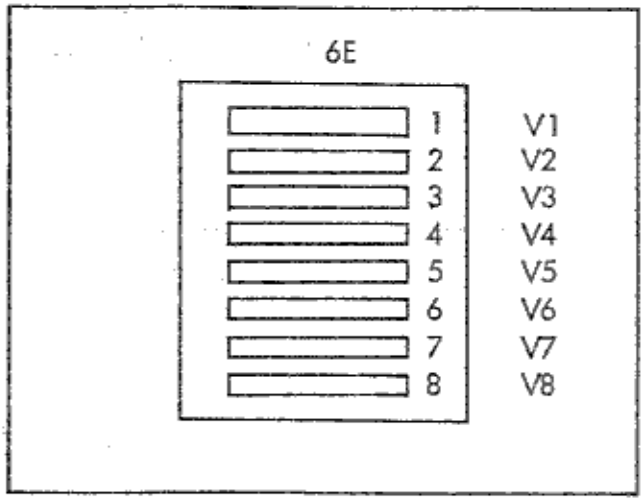
When this is done, whenever a Unibus interrupt is aborted via "grant steal" it will be completed in the Q-bus CPU as an RTI instruction.

The MDB-DWQ module provides the user with the capability to use a 16-pin DIP switch pack for the selection of the "Grant Steal" interrupt vector address. To utilize this feature, perform the following:

a. To be asserted as a "1," place the corresponding switch OPEN.
b. To be asserted as a "0," place the corresponding switch CLOSED.

When using a DIP switch pack, the switches correspond to specific vector address bits, as indicated in Figure 2-1. (If the Grant Steal feature is not used by the Unibus, the position of the switches is insignificant.)

Figure 2-1
"Grant Steal" Interrupt Vector Address Selection



2.2.2 Interpreter at the End of the Q-bus

To install the Interpreter at the end of the bus occupied by the LSI-11-type CPU, perform the following steps:

1. Install jumpers 1 F-H, 2 F-H, 3 F-H, and 4 F-H on the MLSI-DB11 module, and remove jumpers 5F-6F, 5H-6H, 5K-6K, and 5L-6L.

2. Install jumper 3 F-H on the MDB-DWQ module to select an LSI-11 Q-bus CPU. In addition, jumpers 1 F-H, 1 H-J, 2 F-H, and 2 H-J should be removed. (Refer to the note on the following page for the appropriate configuration of jumper 4 F-H.)

3. Remove the NPR jumper (CA1 to CB1) from the first slot of the Unibus backplane.

4. Install the MDB-DWQ module in the first SPC slot of the Unibus backplane. (No Unibus CPU may be used in this configuration.)

   The MDB-DWQ provides termination for the beginning of the Unibus only; a separate terminator is required for the end of the Unibus.

5. Install the MLSI-DB11 module in the last slot of the Q-bus backplane.

   If the Q-bus backplane is terminated on the back side, remove the resistor packs from the MLSI-DB11 module at locations 3A, 7A, and 6C. Note that the MDB MLSI-BPA84-T backplane is terminated with a plug-in terminator assembly on the backplane pins at slot 8 A-B.

6. Connect the 10-foot 60-pin cable between connector P1 of the MDB-DWQ and P1 of the MLSI-DB11.

7. Connect the 10-foot 26-pin cable between P2 of the MDB-DWQ and P2 of the MLSI-DB11.

   Note: The 10-pin cable is not used in this configuration.

8. When the system is "powered-on," the LED mounted on the edge of the MLSI-DB11 module should be illuminated to indicate ACTIVE. On the MDB-DWQ module, the ON, Q CPU, and Q BM LED's should also be illuminated upon power-up.

For a detailed diagram of cable connections, refer to Installation Drawing 01034004, contained at the end of this manual. For "bus switching" details, refer to Section 3.

Note: You may elect to use only I/O devices on the Unibus "add-on" bus. If no memory is used on the Unibus, the Q-bus CPU is able to address up to 4 megabytes of memory on the Q-bus. Only peripheral I/O cycles (asserting BS7) on the Q-bus will be propogated to the slave Unibus segment.

To enable the Interpreter to allow 4 megabytes of memory to be addressed on the Q-bus, jumper 4 F-H must be installed on the MDB-DWQ module. If the jumper is removed, the address range of the system is limited to 256 K bytes.

2.2.3 Interpreter NOT at the End of the Q-bus

To install the Interpreter in the bus occupied by the LSI-11 Q-bus processor, but NOT at the end of that bus, perform the installation procedures outlined in the previous paragraph (2.2.2), as well as the additional steps listed below.

1. Install jumpers 1 J-H and 2 J-H on the MDB-DWQ module.

2. Install jumper 5H-6H on the MLSI-DB11 module.

3. Remove the termination resistor packs from locations 3A, 6C, and 7A of the MLSI-DB11 module.

4. Install the MLSI-DB11 module in any available Q-bus slot, as opposed to installing it in the last Q-bus slot as in the previous section. (Note that Bus Grant Continuity must be maintained in all backplane slots.)

5. Connect the 10-foot 10-pin interconnection cable between P3 of the MDB-DWQ and P3 of the MLSI-DB11, making sure that the pin 1 markings on the connectors line up.

   Note: All other installation procedures are identical to those listed in paragraph 2.2.2.

2.3 Termination

When configured properly for termination, the Interpreter module installed in the last slot of the main CPU backplane (either Unibus or Q-bus) provides 120 ohm termination for the main bus.

When configured for termination, the Interpreter module installed in the first slot of the "add-on" bus (either Unibus or Q-bus) provides 120 ohm termination for the beginning of the add-on bus only. A separate terminator is required at the end of the add-on bus to provide complete termination.

SECTION THREE
SWITCH CONTROL COMBINATIONS

3.0 Introduction

This section provides instructions and information for using the Bus Interpreter in a "Bus Switch" configuration, to permit a common Q-bus to be shared between a PDP-11 Unibus processor and LSI-11 Q-bus processors. There are numerous switching methods available to the user (i.e., manual control, program control). The switching method that is actually utilized is dependent upon user requirements and desires. The most common switch control combinations are described in the following paragraphs. (For more "Bus Switch" details, refer to the MLSI-DB11-S Series of Q-bus Switch Assemblies Instruction Manual.)

The shared bus may be switched from one CPU to another while both CPU's are executing programs, providing no access is made to the devices on the shared bus during the actual switching operation. The CPU that is newly connected to the shared bus should momentarily be HALTED during the switching operation to allow full synchronization.

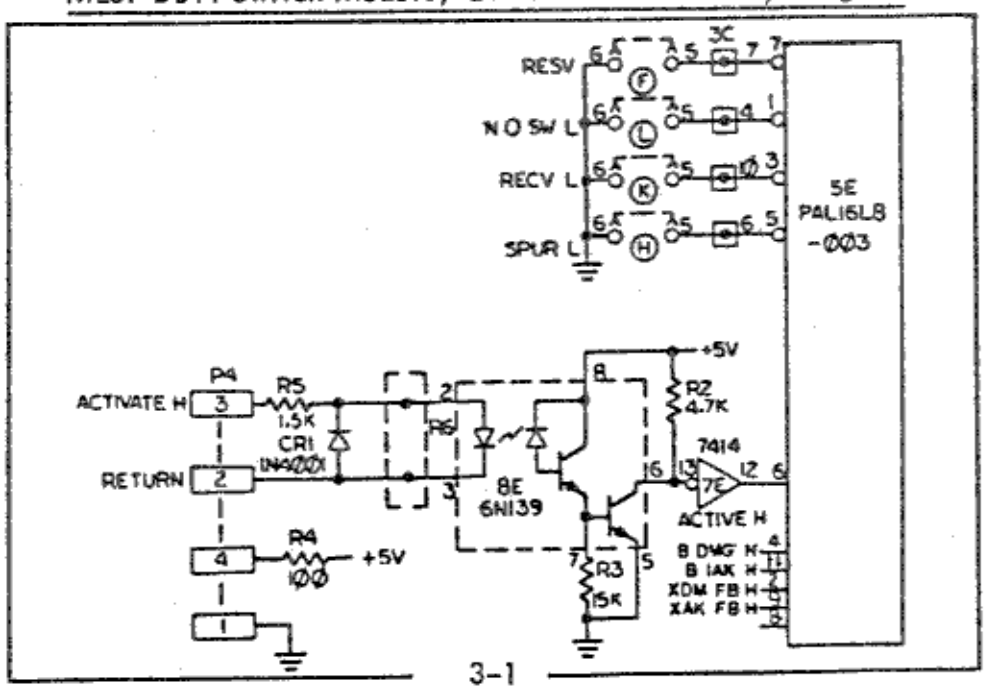
Note: No more than one (1) CPU at a time must ever be connected (selected) to the shared bus or system errors will occur.

When the Bus Interpreter is used as a "bus switch," the MLSI-DB11 module is installed in the shared Q-bus backplane. The status (ON or OFF) of this module determines whether or not the PDP-11 processor may gain access to the Q-bus peripherals on the shared bus.

3.1 Turning the Switch Module ON and OFF

The illustration below shows the circuitry for turning the MLSI-DB11 module ON and OFF, taken from Schematic Diagram No. 44040267, page 2 of 2.

Figure 3-1
MLSI-DB11 Switch Module, ON and OFF Circuitry Diagram



Connector P4 is a 10-pin connector which provides connection to an optically isolated input which causes the MLSI-DB11 module (40040267) to turn either "on" or "off." When the light emitting diode (LED) in the optical isolator (6N139) is forward biased and driven at 2.0 milliamps or greater, the photodarlington circuit in the optical isolator will conduct. This pulls the input of the 7414 Schmitt trigger (location 7E) towards ground, causing the signal ACTIVE H to be asserted (+3 V).

If there is no connection made to connector P4, pins 2 and 3, or when no current is being driven into the LED, the ACTIVE H signal is not asserted (0 V).

The MLSI-DB11 module will always be "on" when the ACTIVE H signal is NOT asserted, AND there is NO jumper present in location 5L-6L. (This jumper, labeled N.O. SW L, becomes an input to the same array logic chip that is driven by the ACTIVE H signal.) When the ACTIVE H signal is asserted (with the jumper removed), the switch module will be "off."

If the user desires to have the switch module "normally off" when the ACTIVE H signal is NOT asserted, then the N.O. SW L (Normally Off) jumper 5L-6L must be installed. Asserting the ACTIVE H signal (with the jumper installed) will turn the MLSI-DB11 module "on."

3.2 Ground Isolation/Noise Rejection

Since the control input for the switch module is optically isolated, the external circuit which drives the LED in the 6N139 may be connected to connector P4, pins 2 and 3 only, and have NO reference to the ground or +5V potentials of the switch module. This condition provides ground isolation.

Also, since the LED in the optical isolator is current-driven, it provides common mode noise rejection that is common to such circuits.

3.3 Manual Switch Control

External switch closures may be used to accomplish manual control of the bus switch. A source resistor is provided and an integration capacitor is required to de-bounce manual switch inputs. No more than one CPU must ever be selected to the shared bus at a time or SYSTEM ERRORS WILL OCCUR. To avoid selecting more than one CPU at a time, a rotary selector switch or a toggle switch (or similar device) could be used.

Note: It is necessary to HALT CPU operation, and the DMA and interrupt activity on the bus, while changing switch positions.

Section 3.3.1 provides detailed instructions for connecting a toggle switch to the switch modules for manual control of the bus switch assembly. Any type of manual switch may be used, providing it is connected to the switch module as described in the following section.

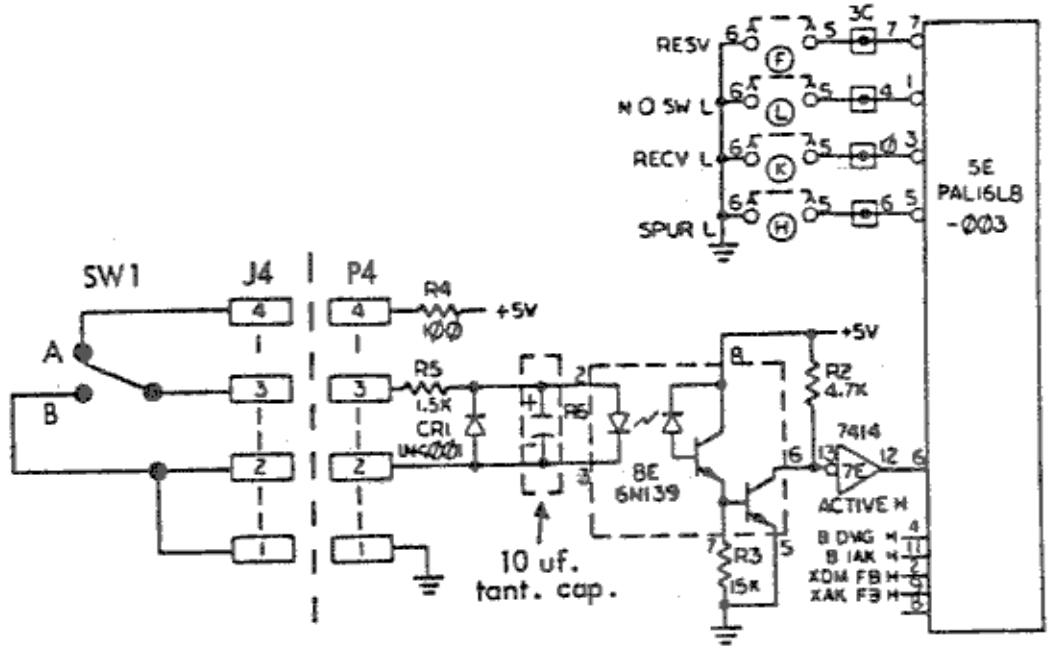
3.3.1 Connecting a Toggle Switch

Use the information provided below to utilize a toggle switch for bus switch control.

Refer to Figure 3-2 and perform the following steps:

1. Connect P4, pin 4, to switch contact A.
2. Connect P4, pin 3, to the switch arm.
3. Connect P4, pins 1 and 2, together and to switch contact B.
4. Install a 10 microfarad polarized tantalum capacitor (rated at 10 V DC or greater) in the optional component space designated R6. This capacitor charges up through resistor R5 and provides switch de-bounce.

Figure 3-2
Utilizing a Toggle Switch for Manual Bus Switch Control



The switch position shown will cause current to flow through the optical isolator (6N139), and assert the ACTIVE H signal.

When the toggle switch (SW1) is placed in the "A" position, +5 volts is impressed upon the control connection pins 2 and 3 (in the proper polarity). This causes about 2 milliamps of current to flow through the LED in the optical isolator (6N139), asserting the signal ACTIVE H, after the capacitor charges up through resistor R5.

When the toggle switch is placed in the "B" position, the user-installed capacitor is discharged through resistor R5 to the ground provided by SW1, causing the LED in the optical isolator to turn off, which de-asserts (negates) the ACTIVE H signal.

The information provided in Table 3-1 shows how to turn the MLSI-DB11 switch module "on" or "off," using the toggle switch in conjunction with the N.O. SW L jumper (5L-6L).

Table 3-1
Turning the Switch Module ON and OFF

Switch Module Status	Jumper 5L-6L	Toggle Switch SW1	ACTIVE H Signal
ON	OUT	Position B	Negated
OFF	IN	Position B	Negated
ON	IN	Position A	Asserted
OFF	OUT	Position A	Asserted

3.4 Program Control from One CPU

A processor in the system can provide the necessary switch system control through use of a digital I/O module (i.e., MDB-DR11-C). The paragraphs below describe how to use a digi I/O module to switch the shared bus between two CPU's through program control.

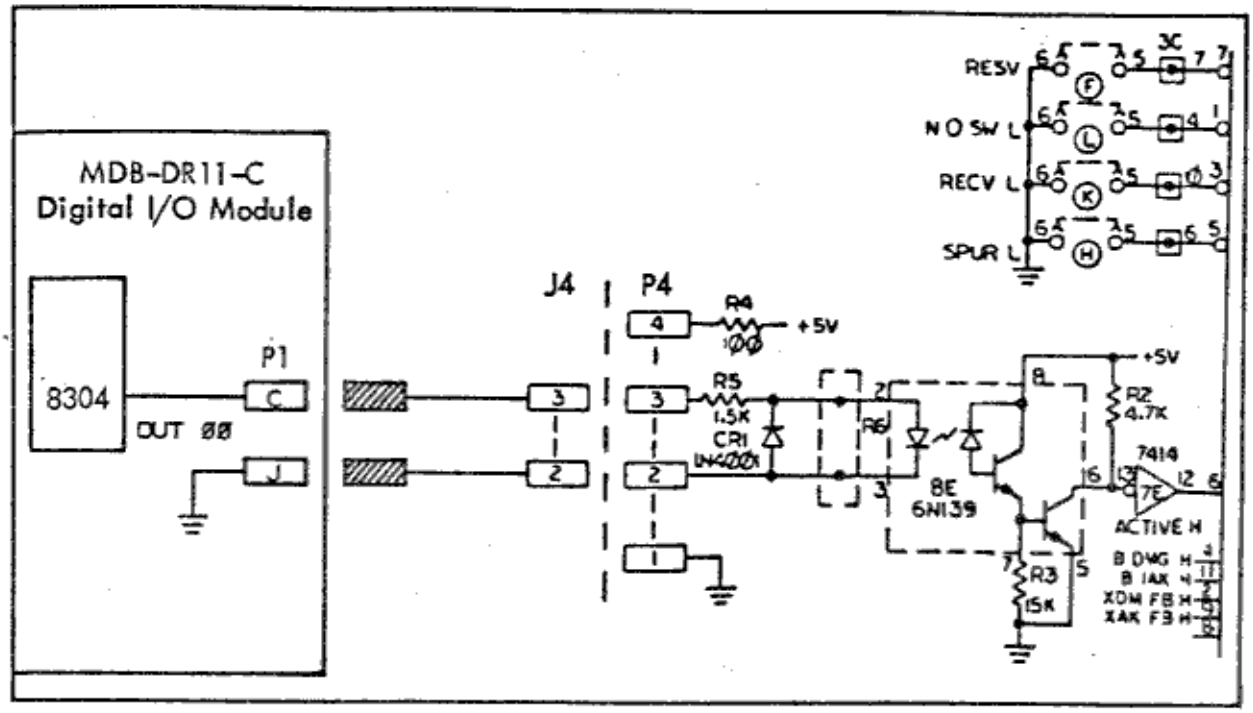
Refer to Figure 3-3 on the following page for MDB/DR11-C/Bus Switch Module connection details.

The output driver of the digital I/O module is connected to P4, pin 3, of the MLSI-DB11 module residing in the shared bus. (The output driver is a tri-state driver with an active pull-up circuit.) A ground pin is connected between the digital I/O module and P4, pin 2, of the MLSI-DB11 module. The output driver and ground pins used for connection to the switch module is determined by user requirements and desires. For example, in Figure 3-3, MDB-DR11-C pins P1, C (Bit 00) and J (ground) are connected to P4, pins 2 and 3, respectively, of the switch module. However, if the user desires, any output driver and ground pin could be used for connection. The example shown is merely a recommendation.

When the Output Data Register is cleared (described on the next page), P4, pin 3, is "pulled-down" to ground (0 volts), negating the ACTIVE H signal.

When the register bit is set, P4, pin 3, is "pulled-up" to 3.5 volts, asserting the ACTIVE H signal.

Figure 3-3
Connection of MDB-DR11-C to Bus Switch Module (Program Control)



The Bus Interpreter is factory-configured so that when no current is sourced into the LED of the optical isolator (either because there are no connections to P4, pins 2 and 3, or there are) volts across pin 2 to 3), the shared bus is automatically connected to the PDP-11 processor. (The switch modules residing in the LSI-11 system backplanes must be turned OFF at this time.)

Bit 00 (P1, pin C) of the MDB-DR11-C's Output Data Register is connected to the switch module installed in the shared bus. Upon power up, the register is cleared and the PDP-11 CPU is connected to the shared bus (the MLSI-DB11 is "on."). To disconnect the shared bus from the PDP-11 CPU, Bit 00 must be set.

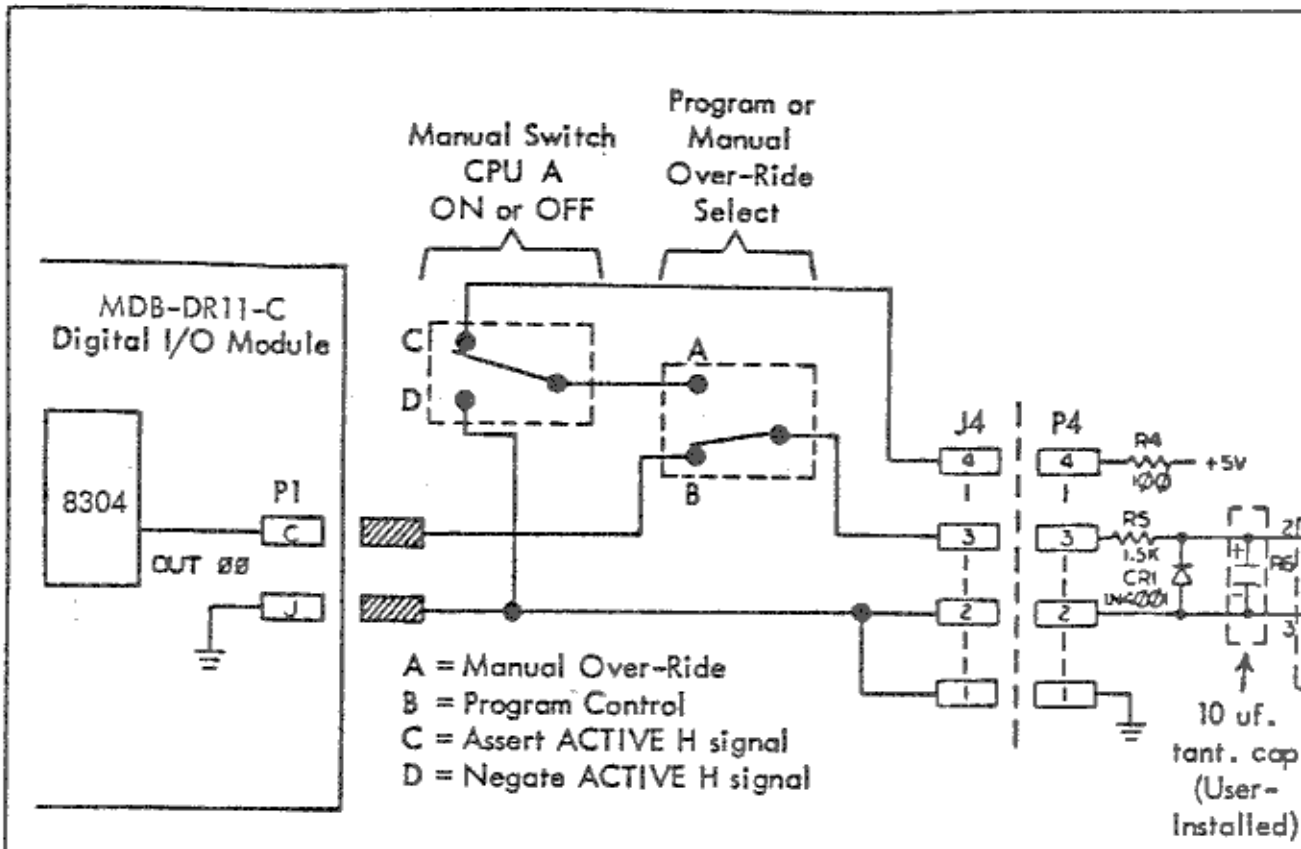
Another CPU can request the shared bus through a serial link. When the PDP-11 is finished with the shared bus, it will switch the bus to the requesting CPU and inform it through the serial link. The PDP-11 will not switch the shared bus back to itself until it makes sure that the other CPU is free to release it. This communication between the CPU's is accomplished through the serial link. This approach requires some software, but can be easily handled through standard drivers.

3.4.1 Program Control with Manual Switch Over-ride

When the switching system is program-controlled, a manual over-ride can be implemented to allow system switching to continue should the programmed I/O module fail.

Refer to Figure 3-4 below. This illustration shows how the MLSI-DB11 switch module receives switch commands from the digital I/O module, unless manual over-ride is selected. Once over-ride is selected, the MLSI-DB11 module will be "on" or "off" as determined by the position of the manual switch.

Figure 3-4
Program Control with Manual Switch Over-ride



(Note: If no external debounce is provided, switch response time increases to ~15msec.

SECTION FOUR
MODULE / BACKPLANE INTERFACES

4.0 General

This section provides a complete listing of bus signals present at the Unibus/MDB-DWQ interface, and signals present at the Q-bus/MLSI-DB11 interface. Refer to the appropriate DEC PDP-11 and LSI-11 documents for detailed timing information and software considerations.

4.1 Unibus/MDB-DWQ Interface

Table 4-1 lists and defines signals at the Unibus/MDB-DWQ module interface. An asterisk (*) denotes a signal that is not used on the MDB-DWQ module.

Table 4-1
Unibus Backplane Interface Terms

Pin	Signal	Description
	D00L-015L	Unibus bidirectional data lines. Low (ground) level is true, +3V is false.
CS2	D00L	Data bit 0 (LSB)
CR2	D01L	Data bit 1
CU2	D02L	Data bit 2
CT2	D03L	Data bit 3
CN2	D04L	Data bit 4
CP2	D05L	Data bit 5
CV2	D06L	Data bit 6
CM2	D07L	Data bit 7
CL2	D08L	Data bit 8
CK2	D09L	Data bit 9
CJ2	D10L	Data bit 10
CH1	D11L	Data bit 11
CH2	D12L	Data bit 12
CF2	D13L	Data bit 13
CE2	D14L	Data bit 14
CD2	D15L	Data bit 15
	A00L-A17L	Device and function address from master device. Low level is true. Bits A01L, A02L, A03L, and control line C1L encode one of 16 addresses. Bits A04L through A17L are used to enable the decoder.

Table 4-1
Unibus Backplane Interface Terms

Pin	Signal	Description
EH2	A00L	Address bit 0 (LSB)
EH1	A01L	Address bit 1
EF1	A02L	Address bit 2
EV2	A03L	Address bit 3
EU2	A04L	Address bit 4
EV1	A05L	Address bit 5
EU1	A06L	Address bit 6
EP2	A07L	Address bit 7
EN2	A08L	Address bit 8
ER1	A09L	Address bit 9
EP1	A10L	Address bit 10
EL1	A11L	Address bit 11
EC1	A12L	Address bit 12
EK2	A13L	Address bit 13
EK1	A14L	Address bit 14
ED2	A15L	Address bit 15
EE2	A16L	Address bit 16
ED1	A17L	Address bit 17
DL1	INITL	Low-level true or negative-going transition received from master device when a programmed RESET instruction is issued, the console START switch is pressed, or a power-up or power-down condition occurs.
EF2	C1L	Control line, low level true. With C0L, specifies the type of cycle to be performed.
EJ2	C0L	Control line, low level true. With C1L, specifies type of cycle to be performed, as follows (0 = unasserted, 1 = asserted): C1L / C0L / Cycle 0 / 0 / DATI 0 / 1 / DATIP 1 / 0 / DATO 1 / 1 / DATOB
EE1	MSYNL	Timing pulse from master device. Negative transition initiates internal timing sequence enabled by address decoding.
EJ1	SSYNL	Negative-going pulse (approx. 200 nsec) sent by module to master device. Follows (by approx. 100 nsec) the negative-going transition of MSYNL when device address has been decoded.

(Table 5-1 is continued on the following page.)

Table 4-1
Unibus Backplane Interface Terms

Pin	Signal	Description
FD1	BBSYL	Busy signal (low level true) sent to master device by interrupt logic on the module. Level falls on receipt of bus grant input, and rises as vector address is transferred onto Unibus.
FT2	SACKL	Control level (low level true) sent to master device by interrupt logic to acknowledge receipt of bus grant input. Reset when vector address has been transferred onto Unibus.
FJ1	NPRL	Bus-master request (low level true) sent by user device to master device.
FM1	INTRL	Control level (low level true) sent to master device by interrupt logic as vector address is transferred onto Unibus.
DH2	BR4L	One of four possible bus request levels sent to master device in response to request by user device. Level is selected by means of wire jumper. Negative level is true.
DF2	BR5L	Bus request level 5 (see BR4L).
DE2	BR6L	Bus request level 6 (see BR4L).
DD2	BR7L	Bus request level 7 (see BR4L).
DS2	BG4INH	One of four possible bus grant input levels sent by master device in response to bus request. Level is selected by means of wire jumper. High level is true.
DP2	BG5INH	Bus grant level 5 (see BG4INH).
DM2	BG6INH	Bus grant level 6 (see BG4INH).
DK2	BG7INH	Bus grant level 7 (see BG4INH).
DT2	BG4OUTH	One of four possible bus grant output levels selected by wire jumper and sent to another controller to extend a serial interrupt priority link. High level is true.
DR2	BG5OUTH	Bus grant output level 5 (see BG4OUTH).
DN2	BG6OUTH	Bus grant output level 6 (see BG4OUTH).
DL2	BG7OUTH	Bus grant output level 7 (see BG4OUTH).

(Table 5-1 is continued on the following page.)

Table 4-1
Unibus Backplane Interface Terms

Pin	Signal	Description
CA1	NPRGINH	Bus-master bus grant signal sent by the master device to the user device in response to NPRL. High level is true.
CB1	NPRGOUTH	Bus-master bus grant output level to another controller to extend serial priority bus-master control. High level is true.
CV1	ACLO L	Power monitoring status to the processor.
CC1	PA L	Device parity error signal.
CS1	PB L	Device parity error signal.
*AA2 *BA2 CA2 DA2 EA2 FA2	+5 V	Power supply from the backplane.
*AC2 *BC2 CC2 DC2 EC2 FC2 *AT1 *BT1 CT1 DT1 ET1 FT1	GND	Signal ground.

4.2 Q-bus/MLSI-DB11 Interface

Table 4-2 lists and defines signals present at the Q-bus/MLSI-DB11 module interface. An asterisk (*) denotes a signal that is not used on the MLSI-DB11 module.

Table 4-2
Functional Description of Q-bus Signals

Bus Pin	Mnemonic	Description
AA1 (CA1)	BIRQ5L	Priority Level 5 interrupt request.
AB1 (CB1)	BIRQ6L	Priority Level 6 interrupt request.
AC1 (CC1)	BDAL16L	Extended address bit 16.
AD1 (CD1)	BDAL17L	Extended address bit 17.
*AE1 (CE1)	SSPARE	Spare pin. Not assigned. This pin is available for user connection.
*AF1 (CF1)	SRUNL	Run light signal.
*AH1 (CH1)	SRUNL	Run light signal.
AJ1 (CJ1)	GND	Signal ground.
*AK1 (CK1)	MSPAREA	Maintenance spare. Normally connected to bus pin AL1 (CL1) on the backplane.
*AL1 (CL1)	MSPAREA	Maintenance spare. Normally connected to bus pin AK1 (CK1) on the backplane.
AM1 (CM1)	GND	Signal ground.
AN1 (CN1)	BDMRL	Direct Memory Access (DMA) Request. Asserted by a device to request control of the bus (bus master). If the processor is not the bus master, and it is not asserting BSYNCL, it grants bus master status to the requesting device by asserting BDMGOL. The requesting device responds by negating BDMRL and asserting BSACKL.
AP1 (CP1)	BHALTL	Processor Halt. A device will cause the processor to halt normal program execution by asserting BHALTL.

Table 4-2
Functional Description of Q-bus Signals

Bus Pin	Mnemonic	Description
AR1 (CR1)	BREFL	Memory Refresh. When BREFL is asserted, the processor will perform as memory refresh that forces all dynamic memory devices to be activated for each BSYNCL/BDINL bus transaction.
*AS1 (CS1)	+12B	+12V battery power.
AT1 (CT1)	GND	Signal ground.
*AU1 (CU1)	PSPARE	Power Spare. Not assigned. This pin is not recommended for use.
*AV1 (CV1)	+5B	+5V battery power.
AA2 (CA2)	+5V	+5V DC power.
*AB2 (CB2)	-12V	-12V DC power.
AC2 (CC2)	GND	Signal ground.
*AD2 (CD2)	+12V	+12V DC power.
AE2 (CE2)	BDOUTL	Data Output. Implies that valid data is available on lines BDAL0L through BDAL15L and, with reference to the bus master device, that an output transfer is in process. The slave device that responds to the BDOUTL signal must assert BRPLYL to complete the data transfer.
AF2 (CF2)	BRPLYL	Reply. Asserted in response to BDINL or BDOUTL. The signal indicates that input data is available on the BDAL bus, or that output data has been accepted from the bus.
AH2 (CH2)	BDINL	Data Input. When BSYNCL is asserted, BDINL indicates an input transfer from the active bus master. When BSYNCL is not asserted, it implies that an interrupt operation is in process.
AJ2 (CJ2)	BSYNCL	Synchronize. Asserted by the bus master device when it has placed an address on lines BDAL0L through BDAL21L.

Table 4-2
Functional Description of Q-bus Signals

Bus Pin	Mnemonic	Description
AK2 (CK2)	BWTBTL	Write/Byte. Controls the bus cycle in either of two ways, as follows: 1. Asserted with leading edge of BSYNCL to indicate that an output sequence will follow (DATO or DATOB). 2. Asserted, while BDOUTL is asserted, for byte addressing in a DATOB cycle.
AL2 (CL2)	BIRQ4L	Priority Level 4 interrupt request.
AM2 (CM2)	BIAKIL	Interrupt Acknowledge. Asserted by the processor in response to BIRQL. Causes the device to put an interrupt vector address on the bus.
AN2 (CN2)	BIAKOL	Interrupt Acknowledge Out. Normally asserted to the device having the next-lower priority on the interrupt chain, and appears at BIAKIL input to that device. If the module stores an interrupt request, BIAKOL is negated at the next device.
AP2 (CP2)	BBS7L	Bank 7 Select. Indicates that the address on the bus is for the upper 4K bank. When BSYNCL is asserted, BBS7L will remain active until the addressing of the bus cycle is completed.
AR2 (CR2)	BDMGIL	DMA Bus Grant Input.
AS2 (CS2)	BDMGOL	DMA Bus Grant Output. This processor-generated signal is daisy-chained through all DMA devices on the bus. When asserted, BDGMIL grants bus master status to the DMA device requesting the bus that has the highest priority. If a higher-priority DMA device has no active bus request, BDMGOL passes from that device to the BDMGIL input of the next DMA device. If the higher-priority device has an active bus request, that device inhibits its BDMGOL output. A DMA device requests the bus by asserting BDMRL.
AT2 (CT2)	BINITL	Initialize. Generated by the processor during a power-up or reset operation. Clears all devices on the I/O bus.

Table 4-2
Functional Description of Q-bus Signals

Bus Pin	Mnemonic	Description
AU2 (CU2)	BDAL0L	Bit 0. One of the data/address bus lines used to transfer all address and data information. Bidirectional.
AV2 (CV2)	BDAL1L	Bit 1. Data/Address bit.
BA1 (DA1)	BDCOKH	DC Power OK. Asserted when the DC voltage level is suitable for reliable system operation.
BB1 (DB1)	BPOKH	AC Power OK. Asserted when primary power is within limits assuring reliable system operation.
BC1 (DC1)	BDAL18L	Bit 18. One of the extended address bus lines used to transfer address information.
BD1 (DD1)	BDAL19L	Extended address bit 19.
BE1 (DE1)	BDAL20L	Extended address bit 20.
BF1 (DF1)	BDAL21L	Extended address bit 21.
*BH1 (DH1)	SSPARE	Special spare. Not assigned. This pin is available for user connection.
BJ1 (DJ1)	GND	Signal ground.
*BK1 (DK1)	MSPAREB	Maintenance spare. Normally connected to bus pin BL1 (DL1) on the backplane.
*BL1 (DL1)	MSPAREB	Maintenance spare. Normally connected to bus pin BK1 (DK1) on the backplane.
BM1 (DM1)	GND	Signal ground.
BN1 (DN1)	BSACKL	Bus Grant Acknowledge. Asserted by a DMA device in response to the processor's BDMGOL signal, indicating that the device is now the bus master.
BP1 (DP1)	BIRQ7L	Priority Level 7 interrupt request.
BR1 (DR1)	BEVNTL	External Event Interrupt Request. Using BEVNTL, Line Time Clock interrupts occur every 16-2/3 msec for a 60 Hz line frequency, and every 20 msec for a 50 Hz line frequency.

Table 4-2
Functional Description of Q-bus Signals

Bus Pin	Mnemonic	Description
*BS1 (DS1)	+12B	+12V battery power.
BT1 (DT1)	GND	Signal ground.
*BU1 (DU1)	PSPARE	Power spare. Not assigned. This pin is not recommended for use.
*BV1 (DV1)	+5V	+5V DC power.
BA2 (DA2)	+5V	+5V DC power.
*BB2 (DB2)	-12V	-12V DC power.
BC2 (DC2)	GND	Signal ground.
*BD2 (DD2)	+12V	+12V DC power.
BE2 (DE2)	BDAL2L	Bit 2. One of the data/address bus lines used to transfer all address and data information. Bidirectional.
BF2 (DF2)	BDAL3L	Bit 3. Data/Address bit.
BH2 (DH2)	BDAL4L	Bit 4. Data/Address bit.
BJ2 (DJ2)	BDAL5L	Bit 5. Data/Address bit.
BK2 (DK2)	BDAL6L	Bit 6. Data/Address bit.
BL2 (DL2)	BDAL7L	Bit 7. Data/Address bit.
BM2 (DM2)	BDAL8L	Bit 8. Data/Address bit.
BN2 (DN2)	BDAL9L	Bit 9. Data/Address bit.
BP2 (DP2)	BDAL10L	Bit 10. Data/Address bit.
BR2 (DR2)	BDAL11L	Bit 11. Data/Address bit.
BS2 (DS2)	BDAL12L	Bit 12. Data/Address bit.
BT2 (DT2)	BDAL13L	Bit 13. Data/Address bit.
BU2 (DU2)	BDAL14L	Bit 14. Data/Address bit.
BV2 (DV2)	BDAL15L	Bit 15. Data/Address bit.

SECTION FIVE
INTERFACE CONNECTOR PIN ASSIGNMENTS

5.0 Introduction

This section provides pin assignments and locations for all connectors associated with the Bus Interpreter Assembly. (Refer to Installation Drawing No. 01034004, contained at the end of this instruction manual, for specific cable connection instructions.)

5.1 Connector Pin Assignments

All connectors for the MLSI-DB11 (45040267) module are shown as viewed from the front edge of the module with Pin 1 furthest from the board ejector. All connectors for the MDB-DWQ (45040270) module are shown as viewed from the side edge of the module with Pin 1 closest to the board ejector.

Connector P1
(MLSI-DB11 and MDB-DWQ)

DAL 11 L	1	2	GND
DAL 08 L	3	4	GND
DAL 13 L	5	6	GND
DAL 10 L	7	8	GND
DAL 09 L	9	10	GND
DAL 07 L	11	12	GND
DAL 06 L	13	14	GND
RPLY L	15	16	GND
DAL 12 L	17	18	GND
DAL 15 L	19	20	GND
DAL 05 L	21	22	GND
DAL 04 L	23	24	GND
DAL 14 L	25	26	GND
*DAL 21 L	27	28	GND
*DAL 20 L	29	30	GND
*DAL 19 L	31	32	GND
DAL 00 L	33	34	GND
DAL 03 L	35	36	GND
DAL 01 L	37	38	GND
BS 7 L	39	40	GND
WT BT L	41	42	GND
*DAL 18 L	43	44	GND
DAL 02 L	45	46	GND
SYNC L	47	48	GND
DAL 17 L	49	50	GND
DAL 16 L	51	52	GND
D IN L	53	54	GND
D OUT L	55	56	GND
REF L	57	58	GND
R DM FB L	59	60	GND

Connector P2
(MLSI-DB11 and MDB-DWQ

P OK L	1	14	GND
DMR L	2	15	GND
SACK L	3	16	GND
DC OK L	4	17	GND
INIT L	5	18	GND
*HALT L	6	19	GND
IRQ 5 L	7	20	GND
*EVNT L	8	21	GND
DMG L	9	22	GND
IAK L	10	23	GND
IRQ 4 L	11	24	GND
IRQ 7 L	12	25	GND
IRQ 6 L	13	26	GND

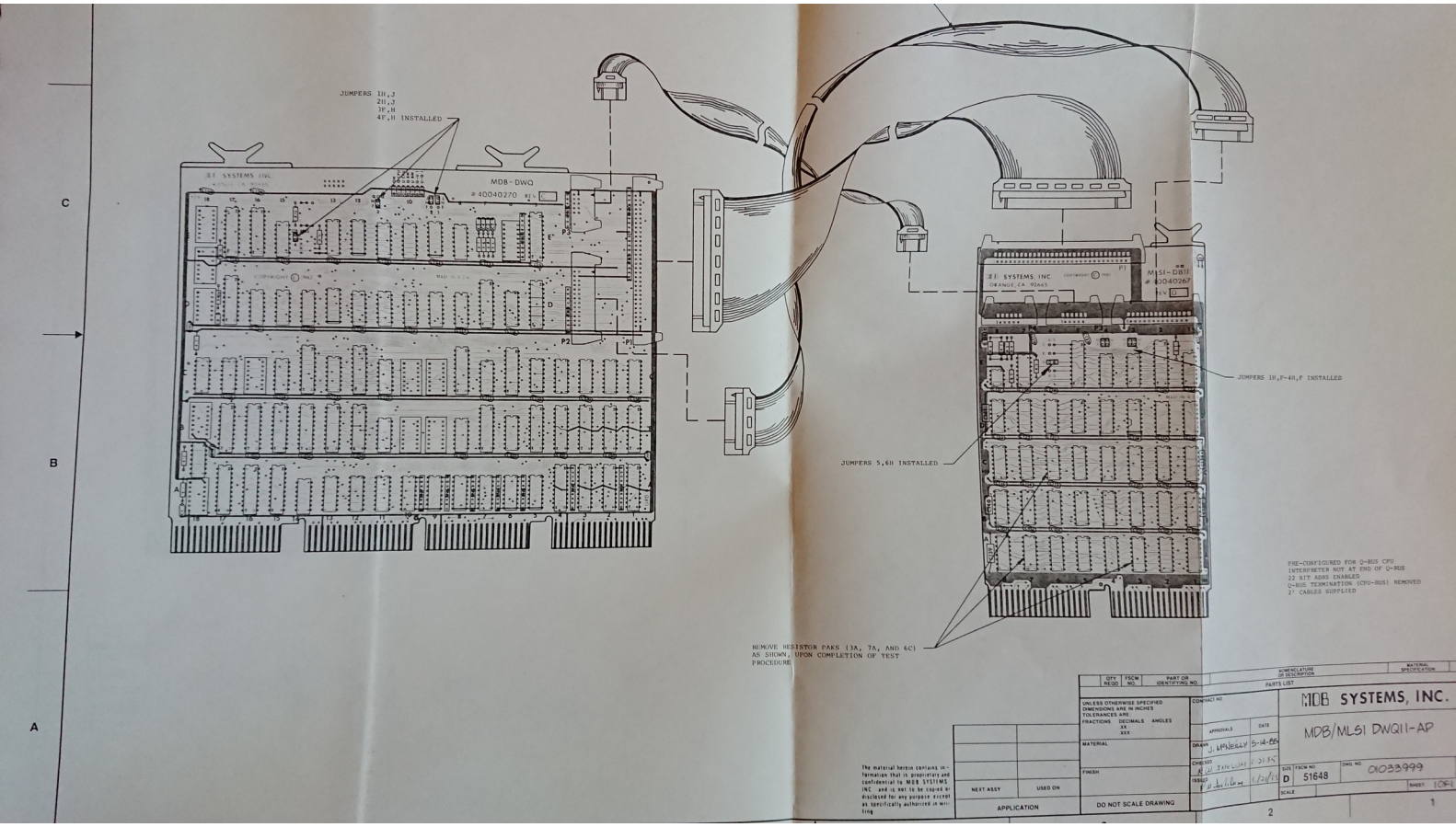
* Signals present on MLSI-DB11 module only.

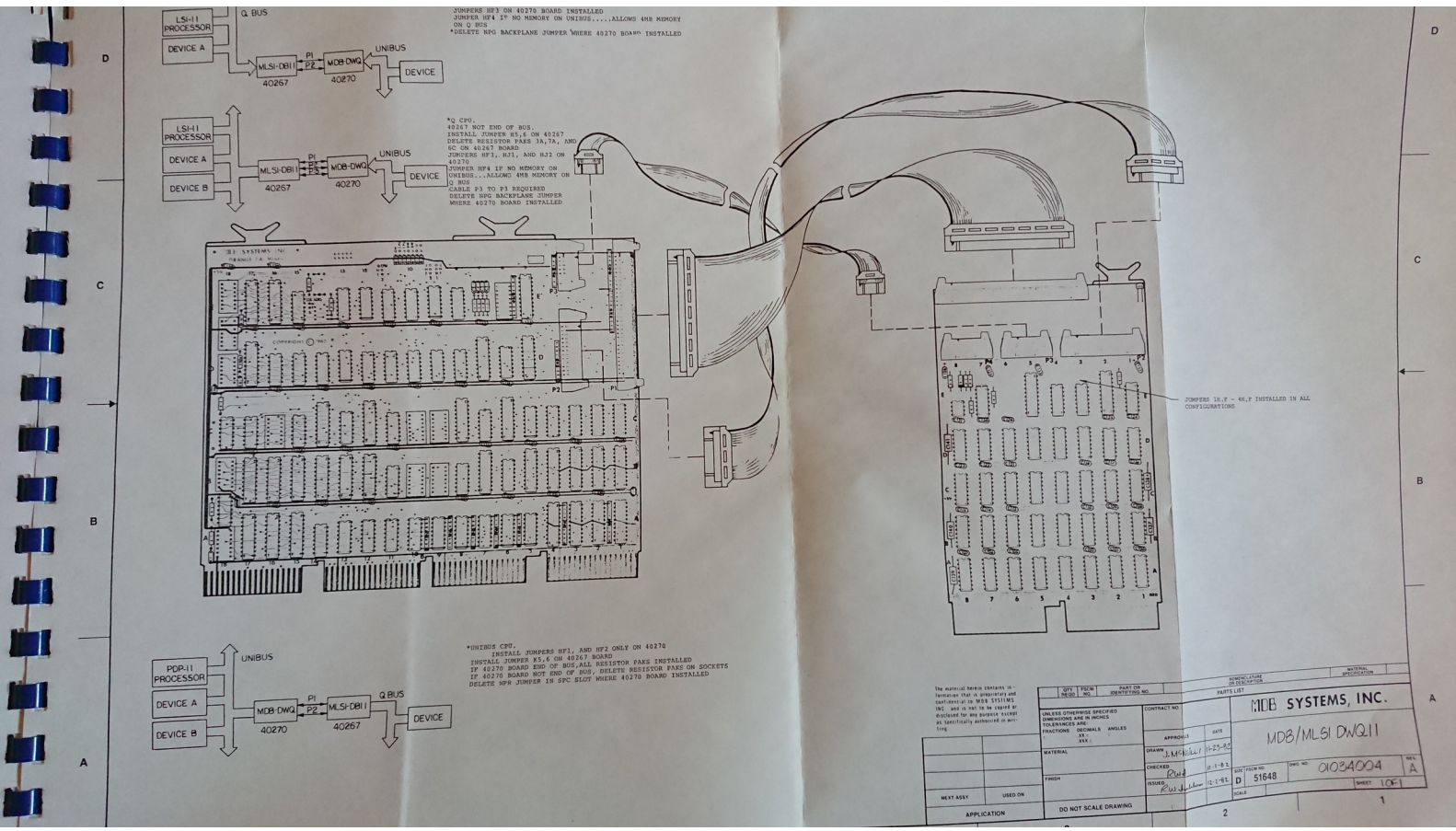
Connector P3
(MLSI-DB11 only)

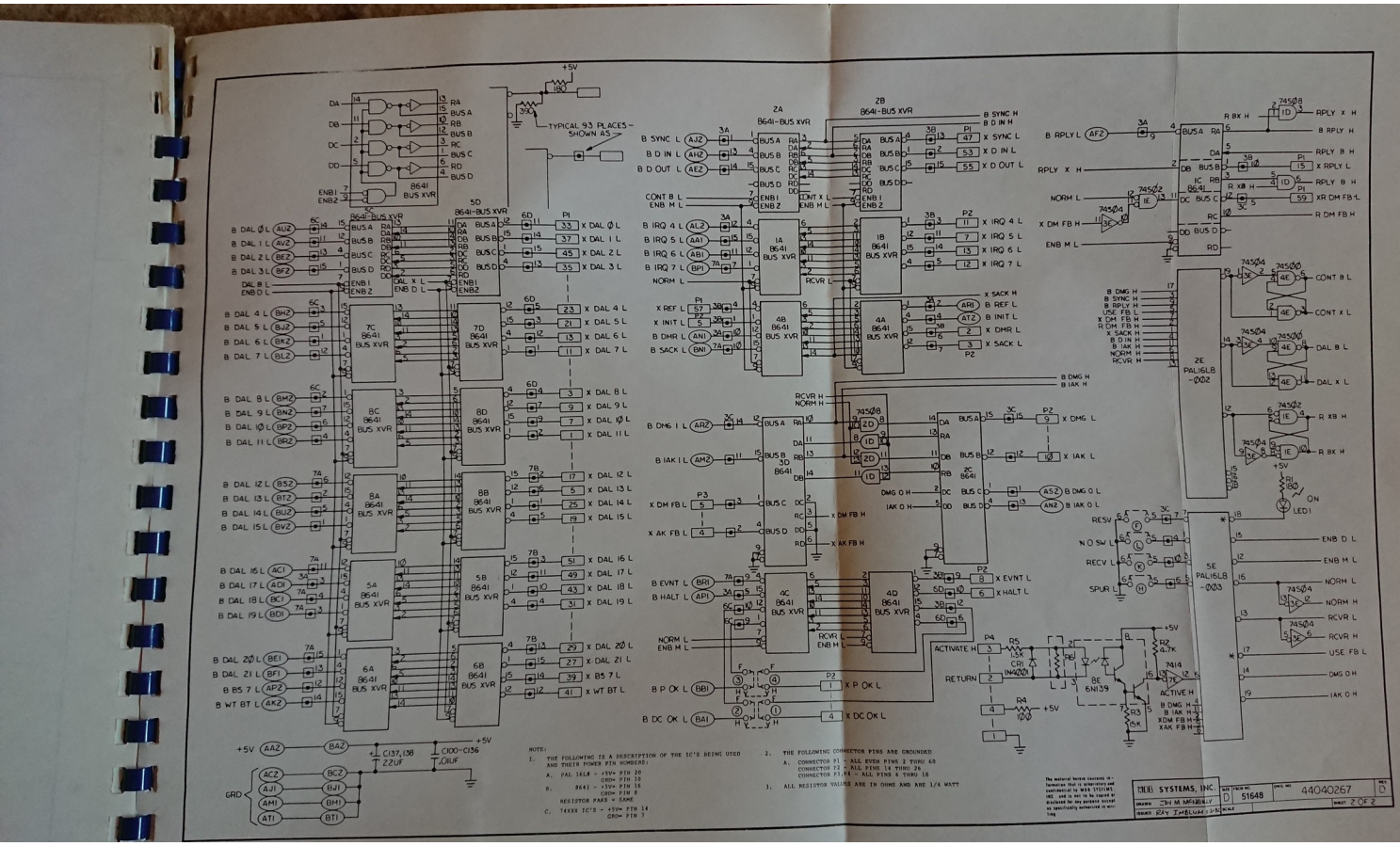
Not Used	1	10	GND
Not Used	2	9	GND
Not Used	3	8	GND
AK FB L	4	7	GND
DM FB L	5	6	GND

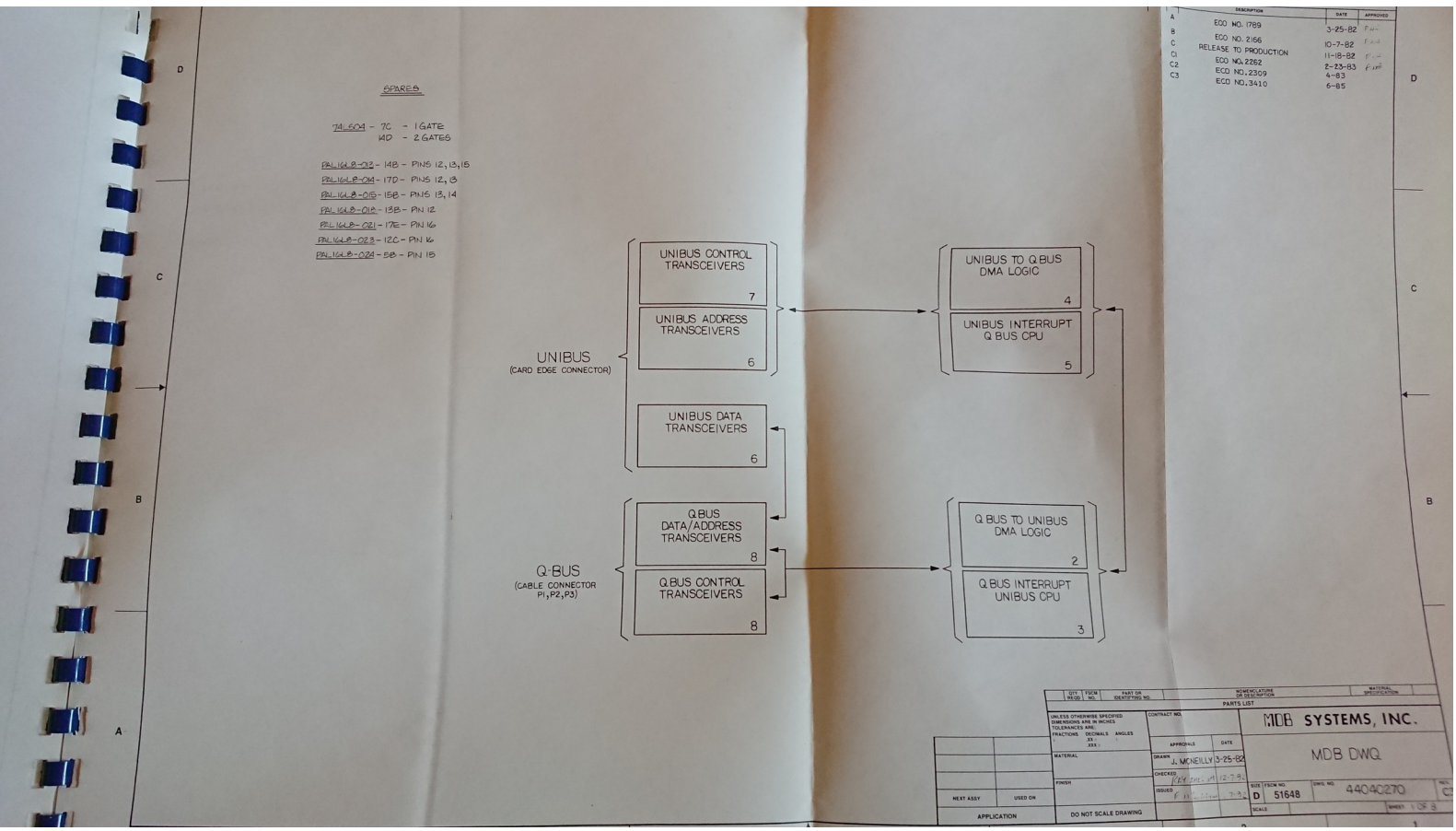
Connector P3
(MDB-DWQ only)

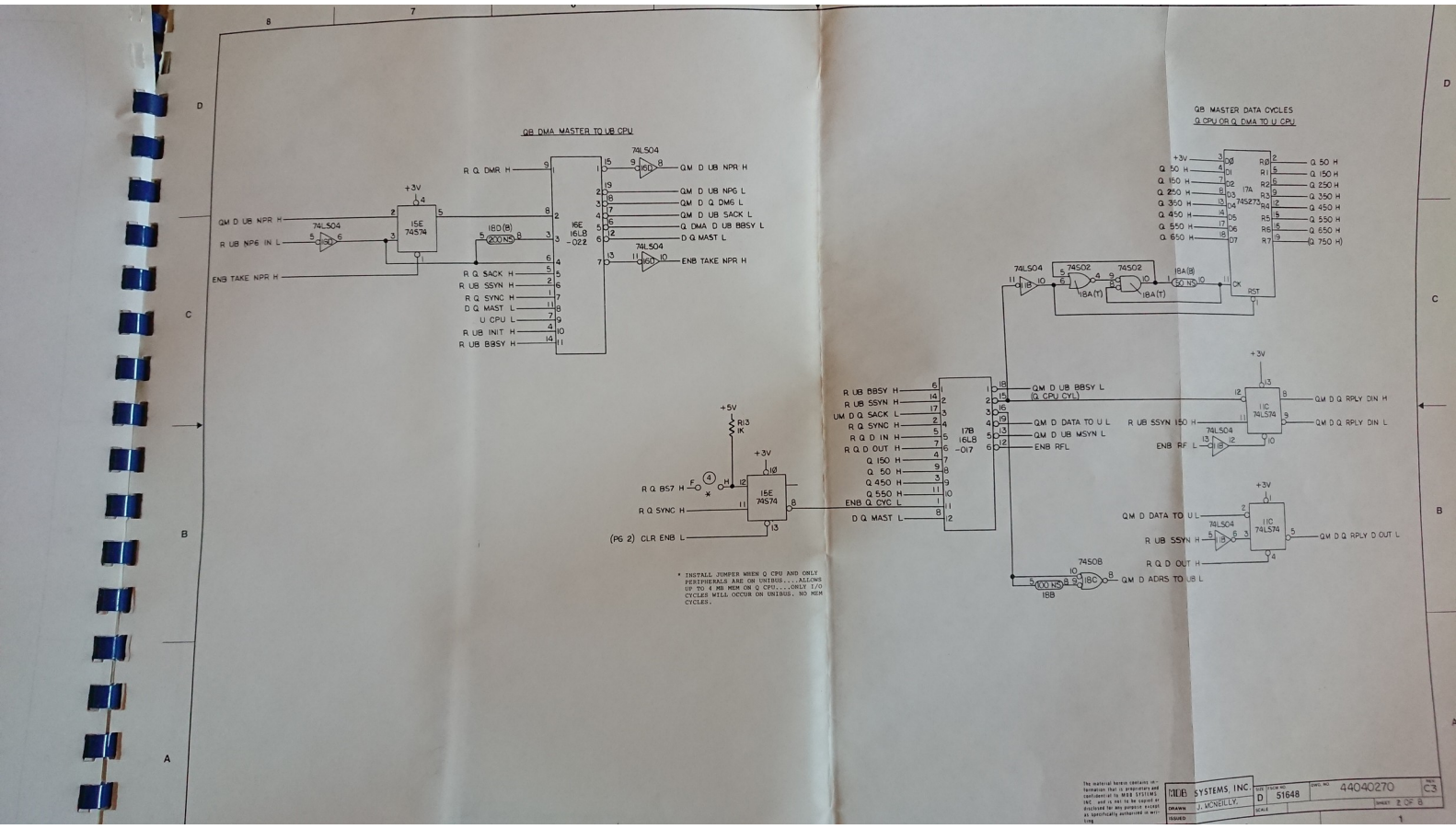
Not Used	1	10	GND
Not Used	2	9	GND
Not Used	3	8	GND
B IAKOL	4	7	GND
B DMGOL	5	6	GND

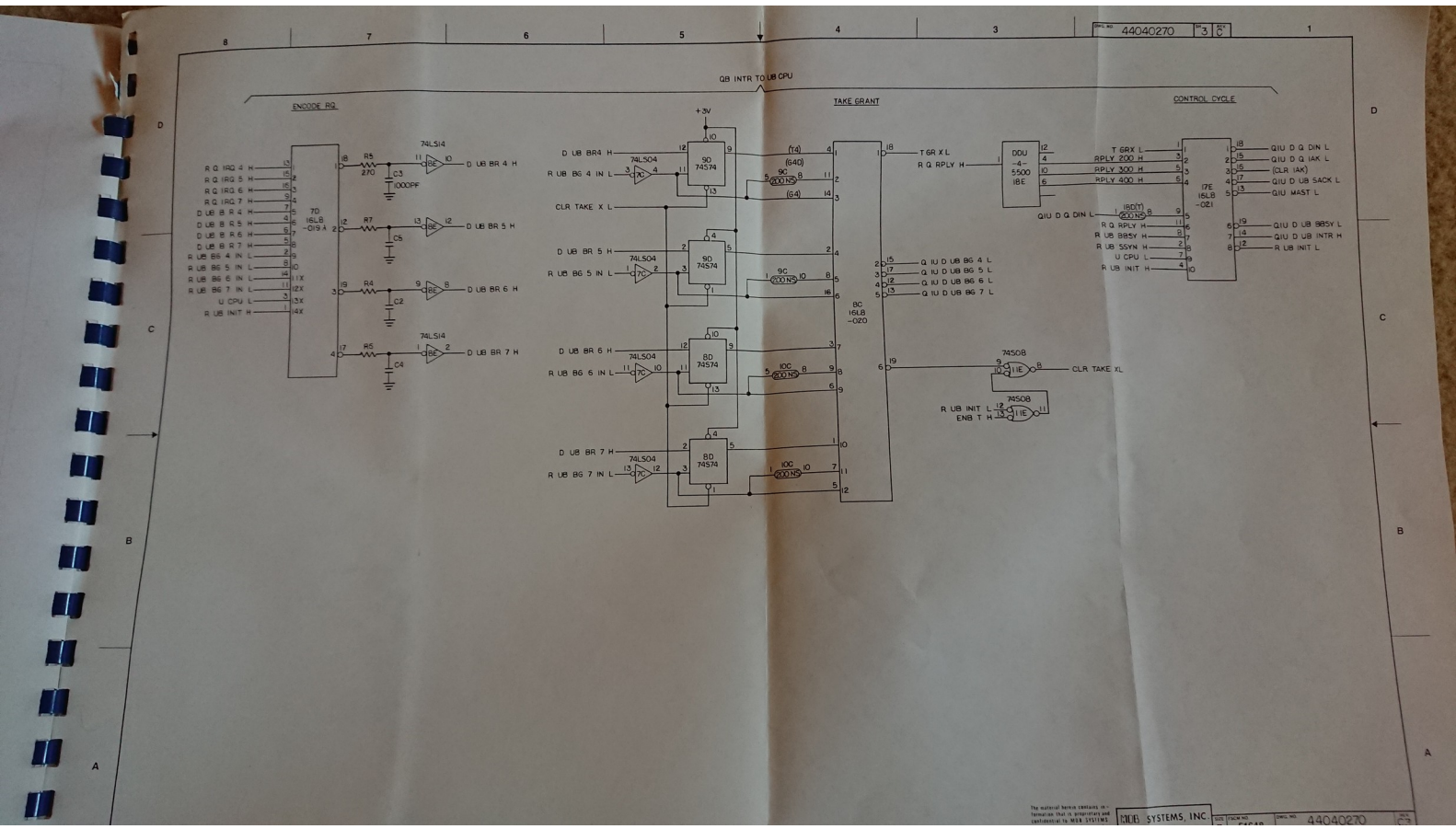

JUMPERS 1H,J
2H,J
3F,H
4F,H INSTALLED
MDB-DWQ
40040270
MLSI-DBII
40040267
JUMPERS 1H,F-4H,F INSTALLED
JUMPERS 5,6H INSTALLED
REMOVE RESISTOR PAKS (3A, 7A, AND 6C) AS SHOWN, UPON COMPLETION OF TEST PROCEDURE
PRE-CONFIGURED FOR Q-BUS CPU
INTERPRETER NOT AT END OF Q-BUS
22 BIT ADRS ENABLED
Q-BUS TERMINATION (CPU-BUS) REMOVED
2' CABLES SUPPLIED
MDB SYSTEMS, INC.
MDB/MLSI DWQ11-AP
01033999
51648

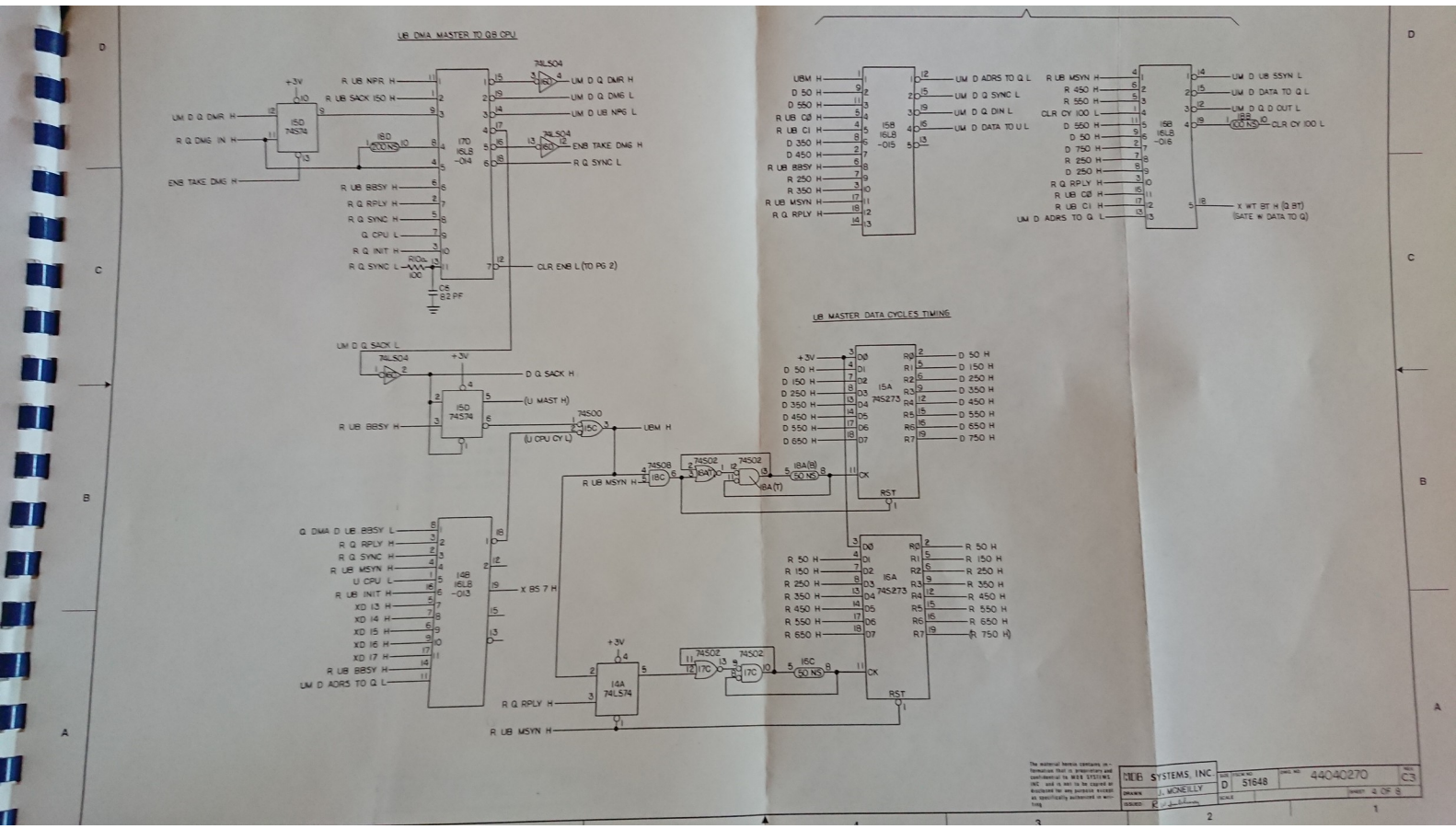

LSI-11 PROCESSOR
DEVICE A
DEVICE B
Q BUS
UNIBUS
DEVICE
MLSI-DBII
MDB-DWQ
40267
40270
JUMPERS HF3 ON 40270 BOARD INSTALLED
JUMPER HF4 IF NO MEMORY ON UNIBUS.....ALLOWS 4MB MEMORY ON Q BUS
*DELETE NPG BACKPLANE JUMPER WHERE 40270 BOARD INSTALLED
*Q CPU.
40267 NOT END OF BUS.
INSTALL JUMPER H5,6 ON 40267
DELETE RESISTOR PAKS 3A,7A, AND 6C ON 40267 BOARD
JUMPERS HF3, HJ1, AND HJ2 ON 40270
JUMPER HF4 IF NO MEMORY ON UNIBUS...ALLOWS 4MB MEMORY ON Q BUS
CABLE P3 TO P3 REQUIRED
DELETE NPG BACKPLANE JUMPER WHERE 40270 BOARD INSTALLED
JUMPERS 1H,F - 4H,F INSTALLED IN ALL CONFIGURATIONS
PDP-11 PROCESSOR
*UNIBUS CPU.
INSTALL JUMPERS HF1, AND HF2 ONLY ON 40270
INSTALL JUMPER K5,6 ON 40267 BOARD
IF 40270 BOARD END OF BUS,ALL RESISTOR PAKS INSTALLED
IF 40270 BOARD NOT END OF BUS, DELETE RESISTOR PAKS ON SOCKETS
DELETE NPR JUMPER IN SPC SLOT WHERE 40270 BOARD INSTALLED
MDB SYSTEMS, INC.
MDB/MLSI DWQ11
01034004
51648

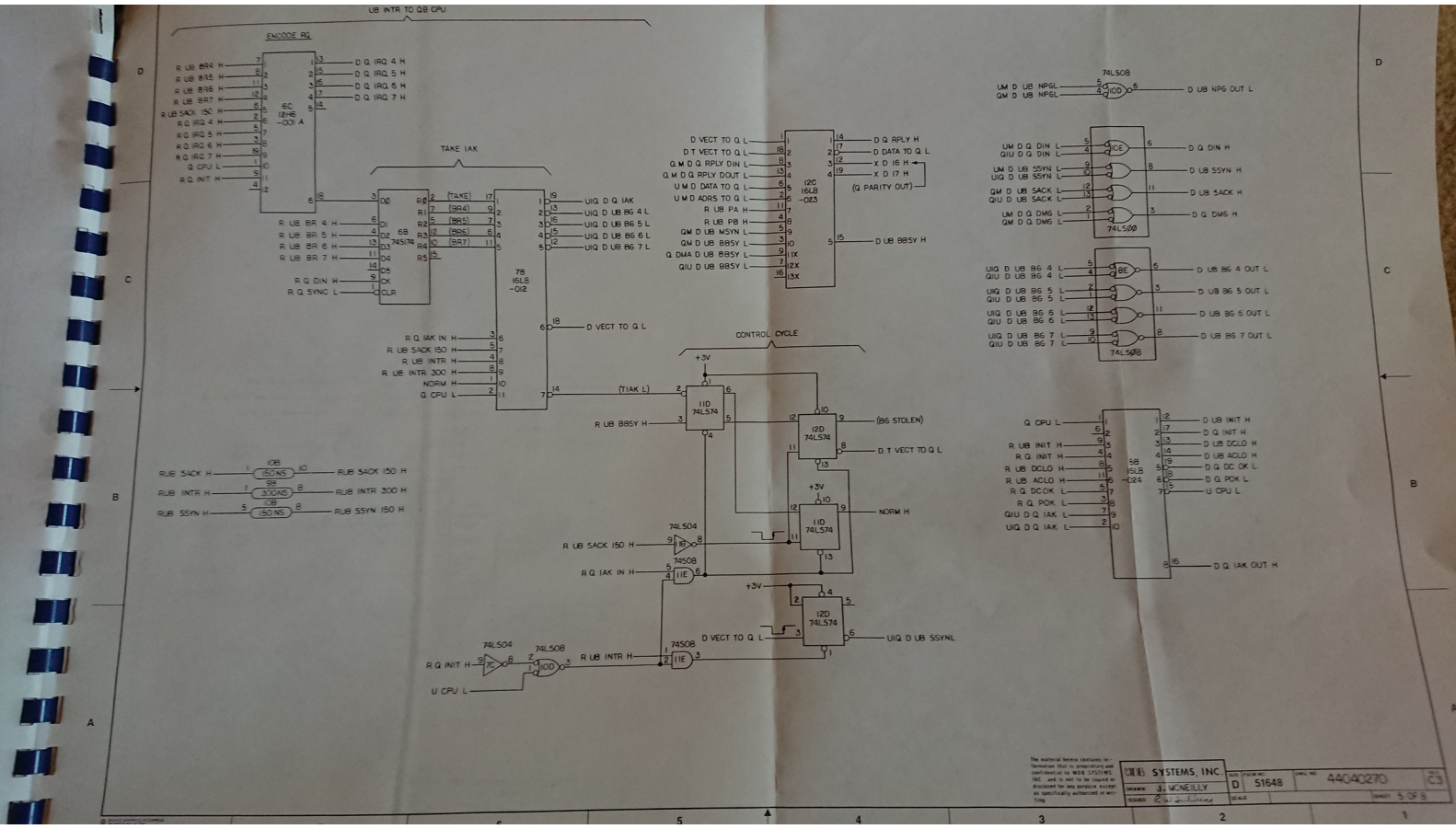

+5V
TYPICAL 93 PLACES SHOWN AS
8641 BUS XVR
ZA 8641-BUS XVR
ZB 8641-BUS XVR
1A 8641 BUS XVR
1B 8641 BUS XVR
4A 8641 BUS XVR
4B 8641 BUS XVR
4C 8641 BUS XVR
4D 8641 BUS XVR
5A 8641 BUS XVR
5B 8641 BUS XVR
5C 8641 BUS XVR
5D 8641-BUS XVR
6A 8641 BUS XVR
6B 8641 BUS XVR
6C 8641 BUS XVR
6D 8641 BUS XVR
7A 8641 BUS XVR
7B 8641 BUS XVR
7C 8641 BUS XVR
7D 8641 BUS XVR
8A 8641 BUS XVR
8B 8641 BUS XVR
8C 8641 BUS XVR
8D 8641 BUS XVR
2E PAL16L8 -002
5E PAL16L8 -003
LED1
MDB SYSTEMS, INC.
44040267

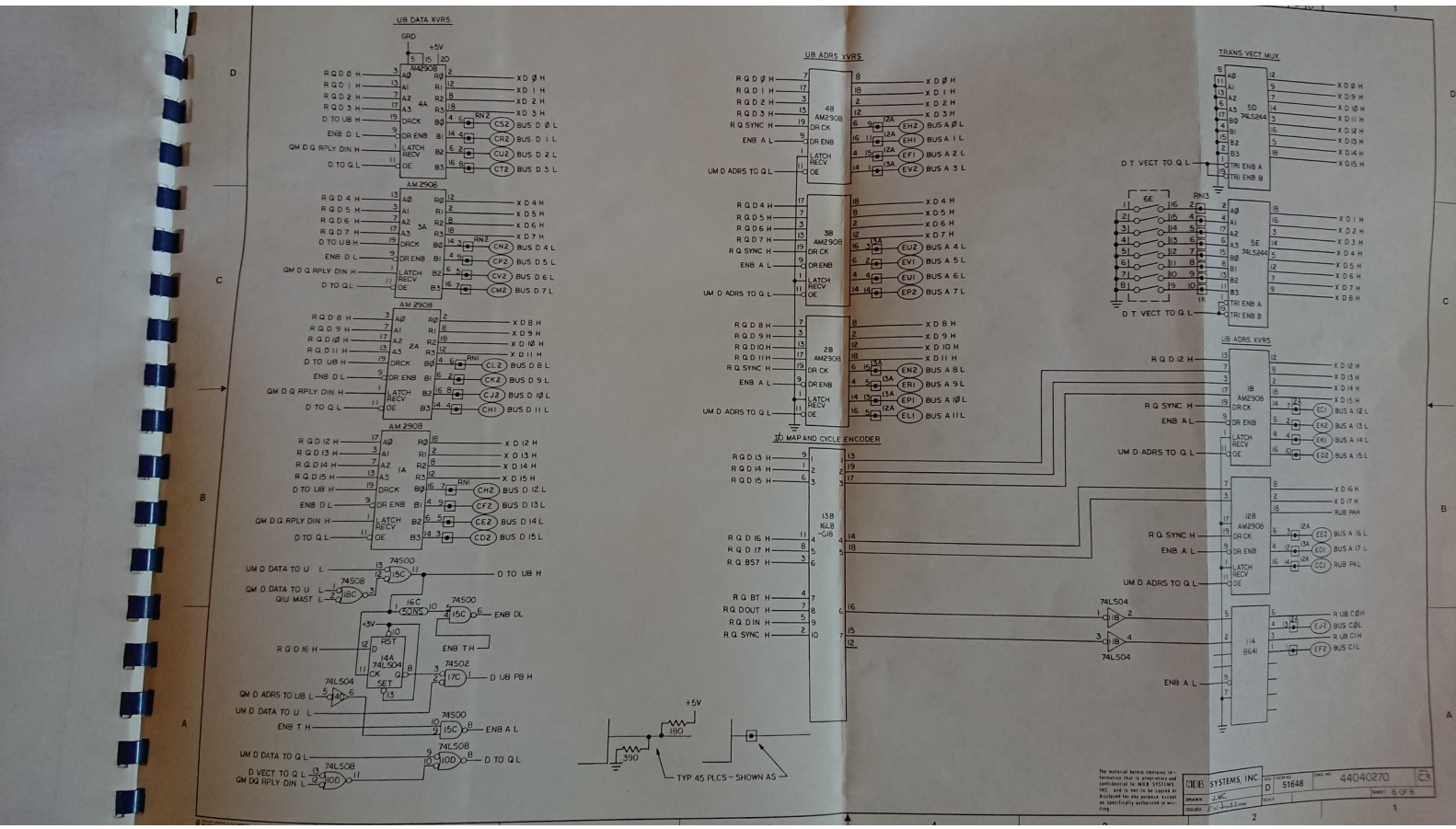

SPARES
74LS04 - 7C - 1 GATE
14D - 2 GATES
PAL16L8-012 - 14B - PINS 12, 13, 15
PAL16L8-014 - 17D - PINS 12, 13
PAL16L8-015 - 15B - PINS 13, 14
PAL16L8-018 - 13B - PIN 12
PAL16L8-021 - 17E - PIN 16
PAL16L8-023 - 12C - PIN 16
PAL16L8-024 - 5B - PIN 15
UNIBUS
(CARD EDGE CONNECTOR)
UNIBUS CONTROL TRANSCEIVERS 7
UNIBUS ADDRESS TRANSCEIVERS 6
UNIBUS DATA TRANSCEIVERS 6
UNIBUS TO Q BUS DMA LOGIC 4
UNIBUS INTERRUPT Q BUS CPU 5
Q-BUS
(CABLE CONNECTOR P1, P2, P3)
Q BUS DATA/ADDRESS TRANSCEIVERS 8
Q BUS CONTROL TRANSCEIVERS 8
Q BUS TO UNIBUS DMA LOGIC 2
Q BUS INTERRUPT UNIBUS CPU 3
ECO NO. 1789
ECO NO. 2166
RELEASE TO PRODUCTION
ECO NO. 2262
ECO NO. 2309
ECO NO. 3410
PARTS LIST
MDB SYSTEMS, INC.
MDB DWG.
44040270


QB DMA MASTER TO UB CPU
QB MASTER DATA CYCLES
Q CPU OR Q DMA TO U CPU
R Q DMR H
QM D UB NPR H
QM D UB NPG L
QM D Q DMG L
QM D UB SACK L
Q DMA D UB BBSY L
D Q MAST L
ENB TAKE NPR H
QM D UB NPR H
R UB NPR IN L
R Q SACK H
R UB SSYN H
R Q SYNC H
D Q MAST L
U CPU L
R UB INIT H
R UB BBSY H
+3V
+5V
R13 1K
R Q BS7 H
R Q SYNC H
(PG 2) CLR ENB L
Q 50 H
Q 150 H
Q 250 H
Q 350 H
Q 450 H
Q 550 H
Q 650 H
(Q 750 H)
R UB BBSY H
R UB SSYN H
UM D Q SACK L
R Q SYNC H
R Q D IN H
R Q D OUT H
ENB Q CYC L
D Q MAST L
QM D UB BBSY L
(Q CPU CYL)
QM D DATA TO U L
QM D UB MSYN L
ENB RFL
R UB SSYN 150 H
ENB RF L
QM D Q RPLY DIN H
QM D Q RPLY DIN L
QM D DATA TO U L
R UB SSYN H
R Q D OUT H
QM D Q RPLY D OUT L
QM D ADRS TO UB L
* INSTALL JUMPER WHEN Q CPU AND ONLY PERIPHERALS ARE ON UNIBUS;...ALLOWS UP TO 4 MB MEM ON Q CPU...ONLY I/O CYCLES WILL OCCUR ON UNIBUS. NO MEM CYCLES.
DEC SYSTEMS, INC
J. MCNEILLY
D
51648
44040270
C3
SHEET 2 OF 8


QB INTR TO UB CPU
ENCODE RQ
TAKE GRANT
CONTROL CYCLE
R Q IRQ 4 H
R Q IRQ 5 H
R Q IRQ 6 H
R Q IRQ 7 H
D UB BR 4 H
D UB BR 5 H
D UB BR 6 H
D UB BR 7 H
R UB BG 4 IN L
R UB BG 5 IN L
R UB BG 6 IN L
R UB BG 7 IN L
U CPU L
R UB INIT H
CLR TAKE X L
T GR X L
R Q RPLY H
Q IU D UB BG 4 L
Q IU D UB BG 5 L
Q IU D UB BG 6 L
Q IU D UB BG 7 L
CLR TAKE XL
R UB INIT L
ENB T H
T GRX L
RPLY 200 H
RPLY 300 H
RPLY 400 H
Q IU D Q DIN L
Q IU D Q DIN H
Q IU D Q IAK L
(CLR IAK)
Q IU D UB SACK L
Q IU MAST L
Q IU D UB BBSY L
Q IU D UB INTR H
R UB INIT L
+3V
DEC SYSTEMS, INC
44040270


UB DMA MASTER TO QB CPU
UB MASTER DATA CYCLES TIMING
UBM H
D 50 H
D 550 H
R UB C0 H
R UB C1 H
D 350 H
D 450 H
R UB BBSY H
R 250 H
R 350 H
R UB MSYN H
R Q RPLY H
UM D ADRS TO Q L
UM D Q SYNC L
UM D Q DIN L
UM D DATA TO U L
R UB MSYN H
R 450 H
R 550 H
CLR CY 100 L
D 750 H
R Q RPLY H
R UB C0 H
R UB C1 H
UM D ADRS TO Q L
UM D UB SSYN L
UM D DATA TO Q L
UM D Q D OUT L
CLR CY 100 L
X WT ST H (Q ST)
(GATE W DATA TO Q)
R UB NPR H
R UB SACK 150 H
UM D Q DMR H
R Q DMG IN H
ENB TAKE DMG H
R UB BBSY H
R Q RPLY H
R Q SYNC H
Q CPU L
R Q INIT H
R Q SYNC L
UM D Q DMR H
UM D Q DMG L
UM D UB NPG L
ENB TAKE DMG H
R Q SYNC L
CLR ENB L (TO PG 2)
C6 82 PF
UM D Q SACK L
D Q SACK H
(U MAST H)
R UB BBSY H
(U CPU CY L)
UBM H
R UB MSYN H
RST
Q DMA D UB BBSY L
R Q RPLY H
R Q SYNC H
R UB MSYN H
U CPU L
R UB INIT H
XD I3 H
XD I4 H
XD I5 H
XD I6 H
XD I7 H
R UB BBSY H
UM D ADRS TO Q L
X BS 7 H
R 50 H
R 150 H
R 250 H
R 350 H
R 450 H
R 550 H
R 650 H
(R 750 H)
R Q RPLY H
R UB MSYN H
D 50 H
D 150 H
D 250 H
D 350 H
D 450 H
D 550 H
D 650 H
D 750 H


UB INTR TO QB CPU
ENCODE RQ
TAKE IAK
CONTROL CYCLE
R UB BR4 H
R UB BR5 H
R UB BR6 H
R UB BR7 H
R UB SACK 150 H
R Q IRQ 4 H
R Q IRQ 5 H
R Q IRQ 6 H
R Q IRQ 7 H
Q CPU L
R Q INT H
D Q IRQ 4 H
D Q IRQ 5 H
D Q IRQ 6 H
D Q IRQ 7 H
R Q DIN H
R Q SYNC L
R Q IAK IN H
R UB INTR H
R UB INTR 300 H
NORM H
D VECT TO Q L
(TIAK L)
UIQ D Q IAK
UIQ D UB B6 4 L
UIQ D UB B6 5 L
UIQ D UB B6 6 L
UIQ D UB B6 7 L
D T VECT TO Q L
Q M D Q RPLY DIN L
Q M D Q RPLY DOUT L
U M D DATA TO Q L
U M D ADRS TO Q L
R UB PA H
R UB PB H
QM D UB MSYN L
QM D UB BBSY L
Q DMA D UB BBSY L
QIU D UB BBSY L
D Q RPLY H
D DATA TO Q L
X D I6 H
X D I7 H
(2 PARITY OUT)
D UB BBSY H
(B6 STOLEN)
R UB BBSY H
R UB SACK 150 H
R Q IAK IN H
D VECT TO Q L
UIQ D UB SSYNL
R Q INIT H
U CPU L
UM D UB NPGL
QM D UB NPGL
D UB NPG OUT L
UM D Q DIN L
QIU D Q DIN L
UM D UB SSYN L
QIU D UB SSYN L
QM D UB SACK L
QIU D UB SACK L
UM D Q DMG L
QM D Q DMG L
D Q DIN H
D UB SSYN H
D UB SACK H
D Q DMG H
UIQ D UB B6 4 L
QIU D UB B6 4 L
UIQ D UB B6 5 L
QIU D UB B6 5 L
UIQ D UB B6 6 L
QIU D UB B6 6 L
UIQ D UB B6 7 L
QIU D UB B6 7 L
D UB B6 4 OUT L
D UB B6 5 OUT L
D UB B6 6 OUT L
D UB B6 7 OUT L
Q CPU L
R UB INIT H
R Q INIT H
R UB DCLO H
R UB ACLO H
R Q DCOK L
R Q POK L
QIU D Q IAK L
UIQ D Q IAK L
D UB INIT H
D Q INIT H
D UB DCLO H
D UB ACLO H
D Q DC OK L
D Q POK L
U CPU L
D Q IAK OUT H


UB DATA XVRS
UB ADRS XVRS
TRANS VECT MUX
UB MAP AND CYCLE ENCODER
TYP 45 PLCS - SHOWN AS
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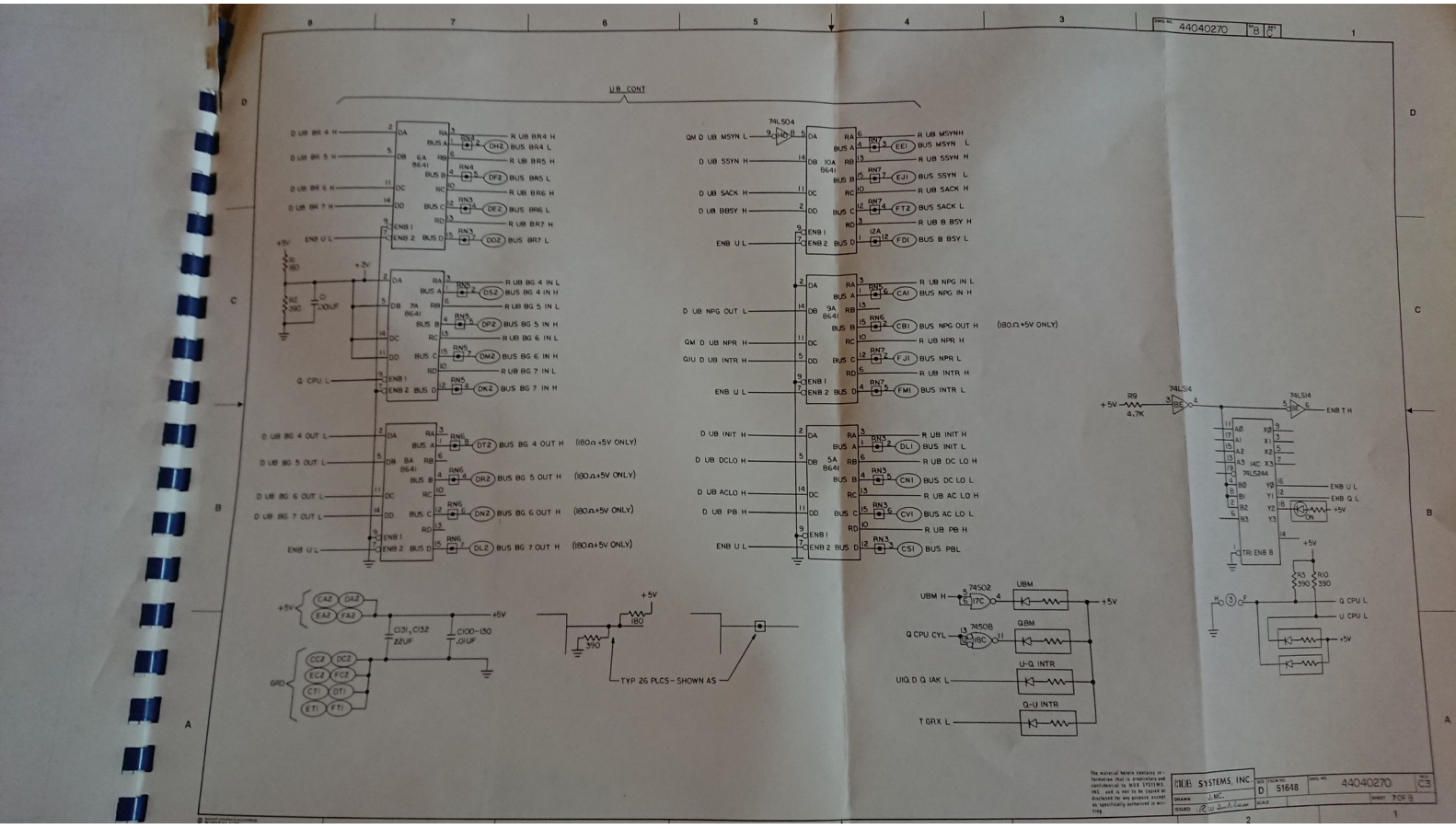
44040270


UB CONT
TYP 26 PLCS - SHOWN AS
(180Ω +5V ONLY)
RIDGE SYSTEMS, INC.
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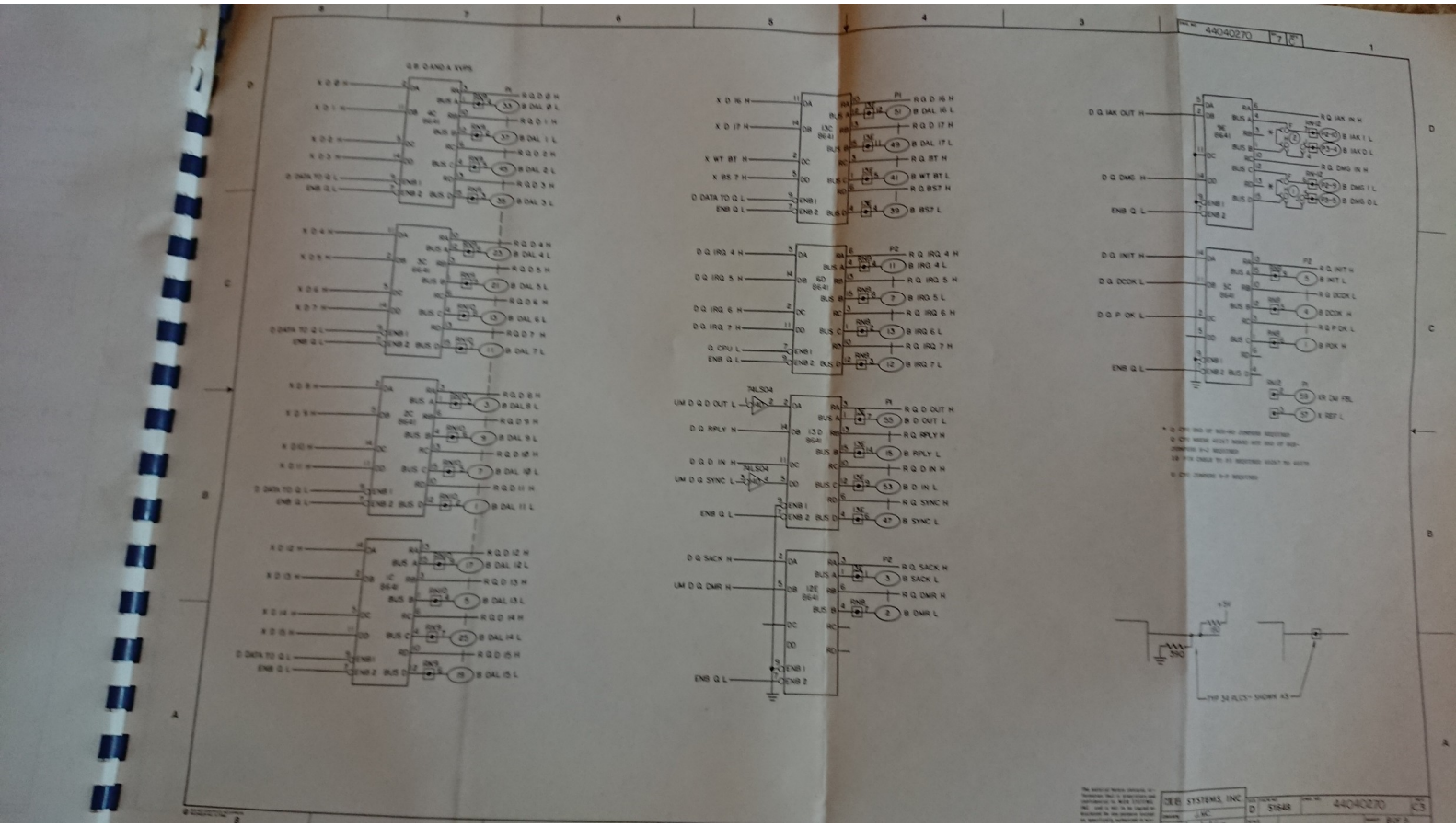

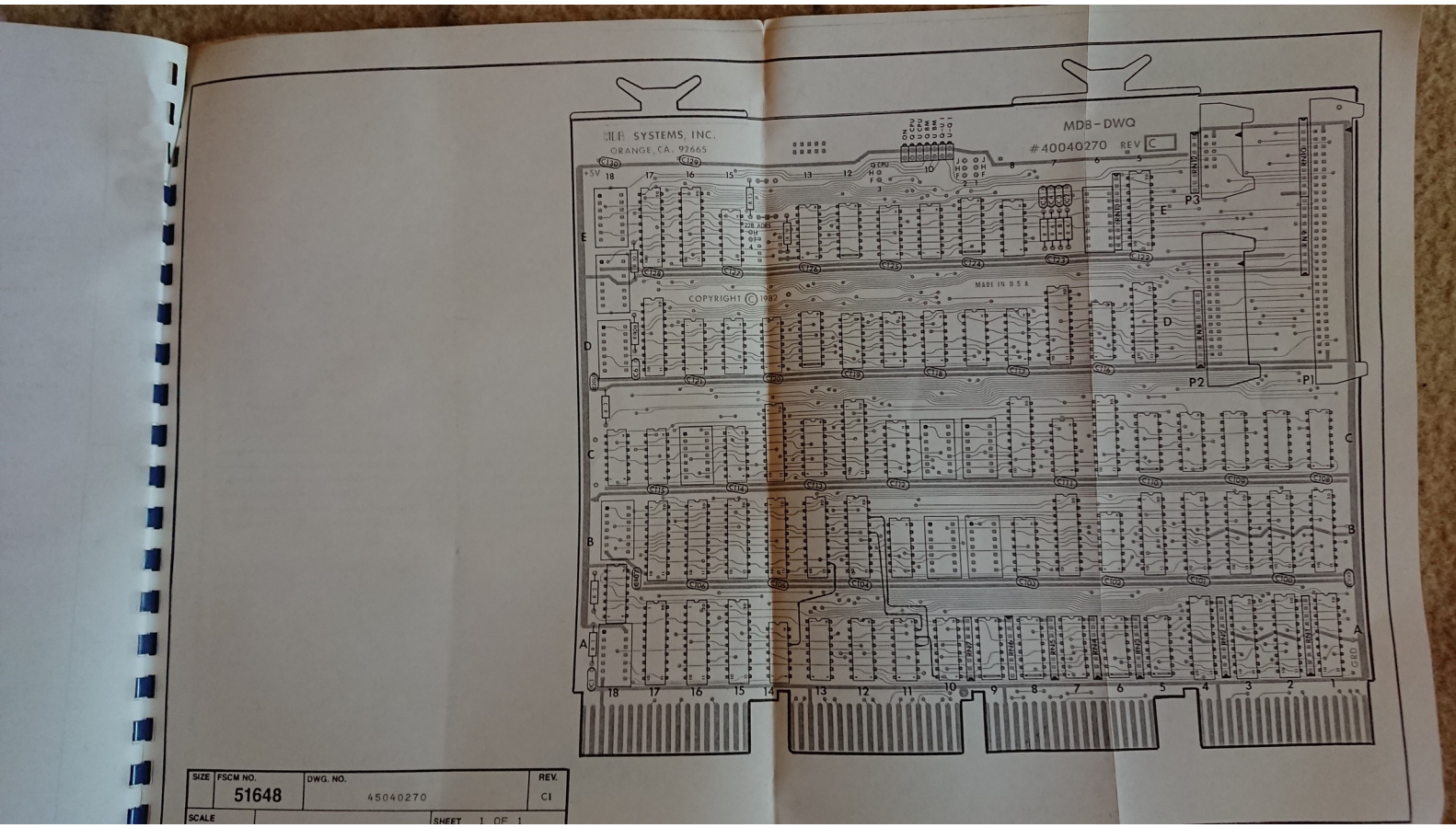
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ORANGE, CA. 92665
MDB-DWQ
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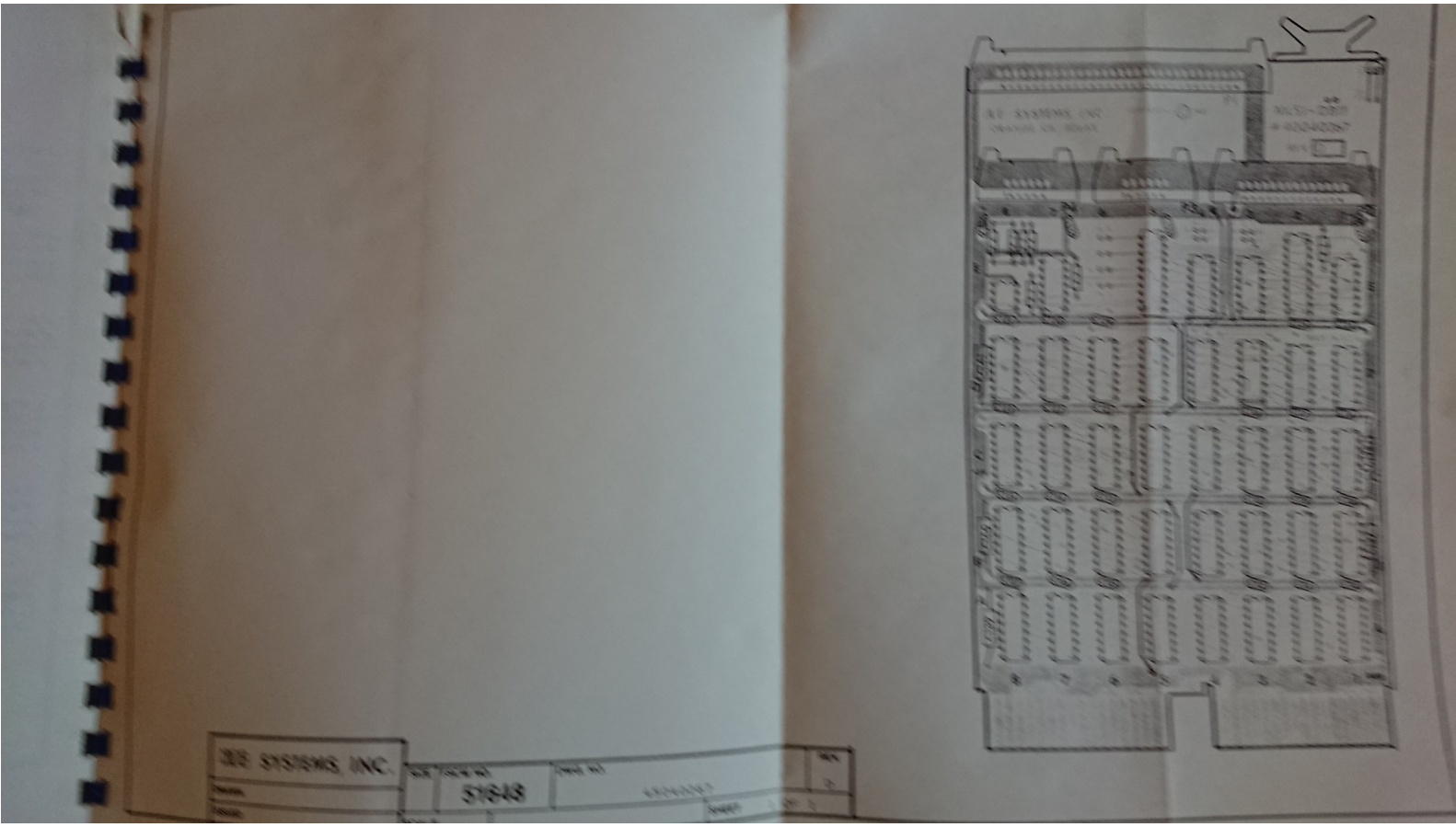
C1
SCALE
SHEET 1 OF 1


3D SYSTEMS, INC.
51643